AUSTRON

AUSTRON INC. P.O. BOX 14766 · EXIT 248, N. IH 35, AUSTIN, TEXAS 78761 (512) 251-2341 TWX 910/874-1356

MODEL 8132-0411

TIME CODE READER

INSTRUCTION MANUAL

SERIAL NO. 1099

NOTICE:

DISREGARD ALL SYSTRON DONNER

ADDRESSES AND TELEPHONE NUMBERS

WARRANTY

AUSTRON, INC., of Austin, Texas, warrants, for one year after delivery, to the original purchaser of any product manufactured by AUSTRON, that same shall be free of defects in material and workmanship. Obligation under this warranty shall be limited to repair or replacement, at AUSTRON's discretion, of any product or part thereof which has been returned by the original purchaser with transportation prepaid, and upon examination by AUSTRON, is found to be defective. AUSTRON assumes no reponsibility for loss or damage to equipment being returned for repair or replacement under the terms of this warranty.

For this warranty to be effective, the purchaser agrees that the equipment will be properly installed and maintained. Equipment which, upon examination by AUSTRON, requires repair or replacement of parts thereof as a result of improper installation, misuse, unauthorized alterations or repairs, or user negligence, such repairs or replacement of parts thereof will be made at cost.

AUSTRON makes no representation or warranty of any kind, either expressed or implied, with respect to equipment operation and procedures. Any action that the user may take in reliance upon the operation or accuracy of this equipment shall be taken solely upon the user's own responsibility and risk.

AUSTRON shall not be liable for consequential damages to purchaser, user, or any others resulting from the possession or use of this equipment.

Prior to return of a product under terms of this warranty, AUSTRON, INC., Austin, Texas, is to be notified. Notification is to include the Model Number and Serial Number of the product and full details of the problem.

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CHAPTER ONE

GENERAL DESCRIPTION

1.1 INTRODUCTION

The Model 8132 Time Code Reader decodes an incoming serial modulated time code. Time information stripped from the input code is displayed and fed, in parallel BCD form, to a rear panel connector. The Time Code Reader incorporates extended range AGC, error bypass, and digital filtering for reliable decoding of the incoming time code.

The basic unit reads an IRIG B time code on a 1 KHz carrier. Time is displayed in hours, minutes and seconds. Four pulse rates (1 pps, 10 pps, 100 pps and 1 Kpps) are supplied as outputs.

Other time codes from the IRIG, NASA and XR3 code families may be substituted for IRIG B as options. The unit can be expanded to include Days/ID Number and to provide parallel BCD outputs representing Days/ID and/or Milliseconds. Other options are also available. (Refer to the standard option list at the front of this manual.)

The Model 8132 is constructed with highly reliable semiconductors and monolithic IC's assembled on printed-circuit, plug-in modules for ease of maintenance.

1.2 SPECIFICATIONS

1.2.1 Display

A 6-digit, in-line, in-plane display indicates time-of-day in hours, minutes and seconds. Day option adds 3-digits. Numeral height is 0.55" (14mm). Colons are provided between seconds and minutes, minutes and hours, and hours and days (when the Days/ID Option is included).

1.2.2 Code Format

IRIG B format, in terms of BCD hours, minutes and seconds (Days/ID optional). Other IRIG, NASA or XR3 code formats are available as options.

1.2.3 Inputs

UPDATE INHIBIT: A +5 V level (or open circuit) enables update. A ground condition delays update. Update may be delayed up to 0.5 ms without losing a count. Via rear panel connector, Amphenol 57-40360.

MODULATED CODE, EXTERNAL: The input modulated code, via a rear panel BNC connector, may have a carrier frequency from 30 Hz to greater than 500 KHz, input levels from 50 mV to 50 V peak-to-peak, and modulation ratios from 2:1 to 6:1. Input impedance is 100 KΩ minimum.

1.2.4 Outputs (Outputs are short-circuit-proof to ground)

PULSE RATES: Simultaneous rates of 1 pps, 10 pps, 100 pps, and 1000 pps are provided with leading edge "on time." Levels are 0 to +5 V (nominal) from a 6 KΩ source (DTL). Connector is rear panel Amphenol 57-40360.

PARALLEL BCD OUTPUTS: Updated time is provided as 24 parallel BCD bits (20 active) representing hours, minutes and seconds. Days/ID option adds 12 bits. Connector is rear panel Amphenol 57-40500.

Code:	8-4-2-1.
Logic:	Binary "1" = 5 ±0.5 volts, behind 6 KΩ. Binary "0" = 0 ±0.5 volts, 12 mA sink.

1.2.5 Environment

Operating:	0°C to +60°C at up to 95% relative humidity.
Storage:	-55°C to +85°C.

1.2.6 Power

115/230 V ±10%, 48 to 62 Hz at less than 60 watts.

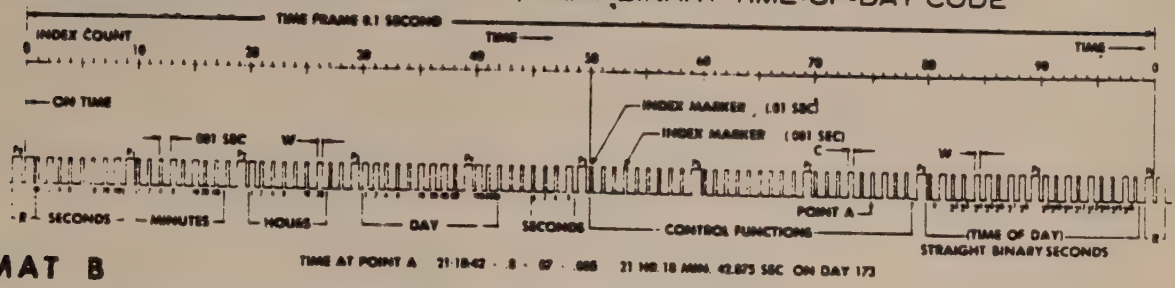
1.2.7 Package

3-½" (8.9 cm) high by 19" wide by 17" (43.1 cm) deep. Removable rack flanges. Chassis drilled for Jonathan 120 QD series slides. Weight approximately 25 lbs (11 kg) net, 35 lbs (16 kg) shipping.

FIGURE 1.1 IRIG TIME CODE FORMATS

FORMAT A

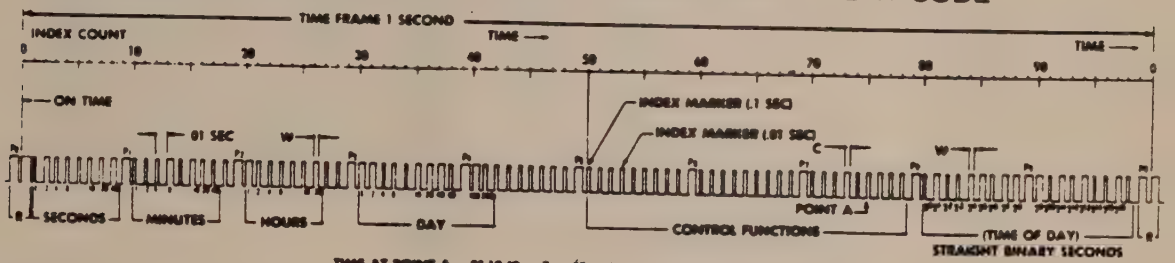
1000-PPS, 34-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A 21:18:42 . 8 . 07 . 008 21 HR. 18 MIN. 42.875 SEC. ON DAY 173

FORMAT B

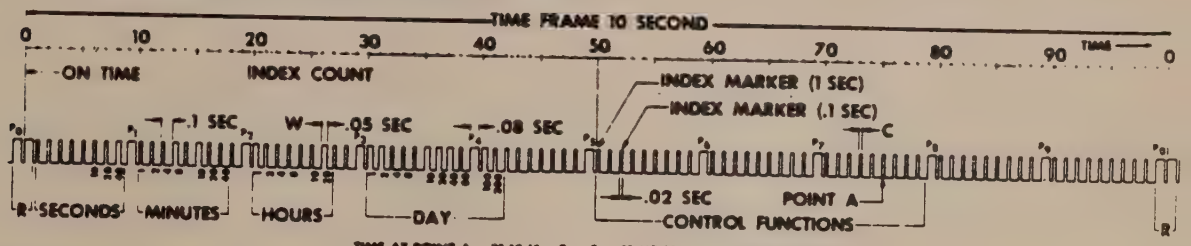
100-PPS, 30-BIT BCD TIME-OF-YEAR/17-BIT BINARY TIME-OF-DAY CODE



TIME AT POINT A - 21:18:42 - .7 - .68 - 21 HRS. 18 MIN. 42.75 SEC. ON DAY 173

FORMAT E

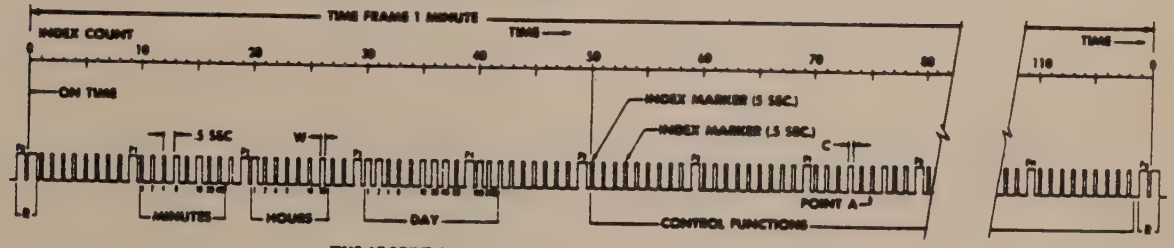
10-PPS, 26-BIT BCD TIME-OF-YEAR CODE



TIME AT POINT A - 21:18:40 - 7 - .5 - 21 HR. 18 MIN. 47.5 SEC. ON DAY 173

FORMAT C

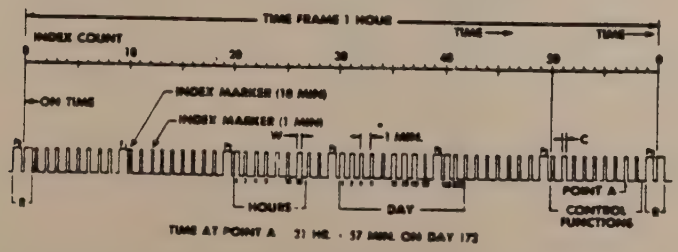
2-PPS, 23-BIT BCD TIME-OF-YEAR CODE



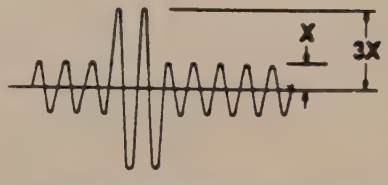
TIME AT POINT A - 21:18 - 37.5 SEC. - 21 HRS. 18 MIN. 37.5 SEC. ON DAY 173

FORMAT D

1-PPM, 16-BIT BCD TIME-OF-YEAR CODE

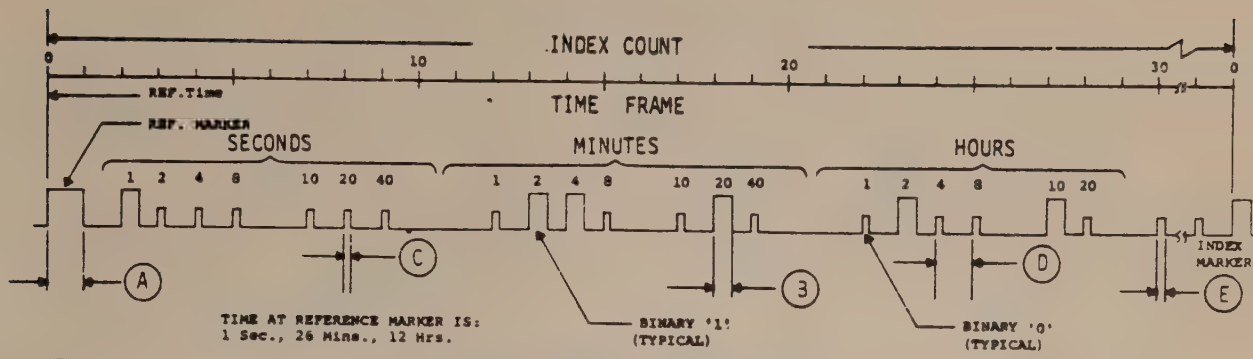


TIME AT POINT A 21 HR. - 57 MIN. ON DAY 173



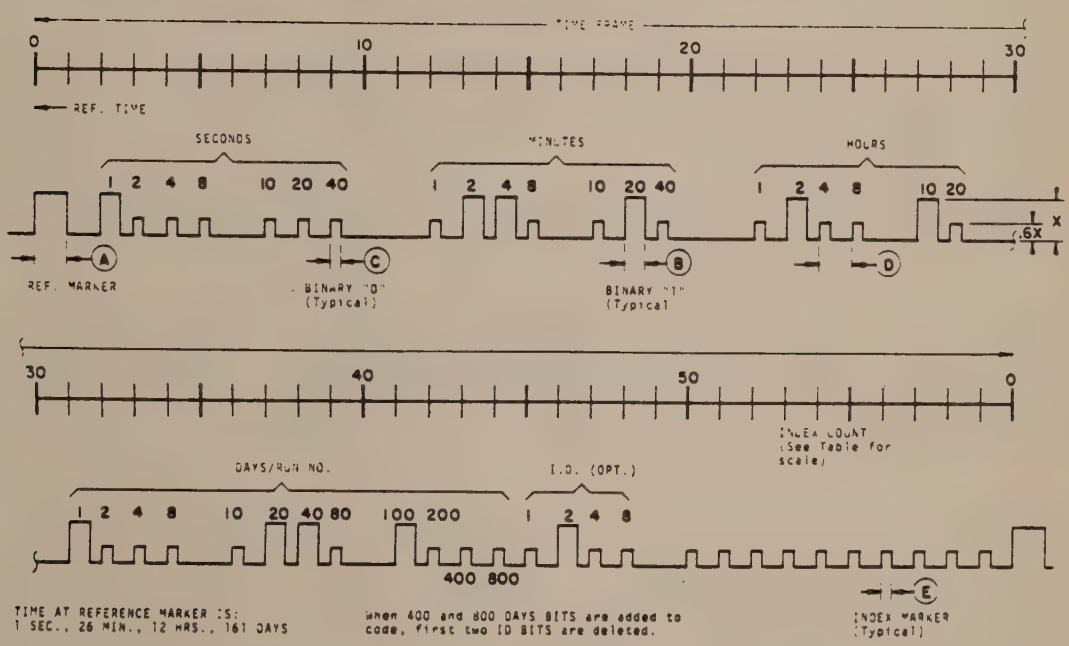
TYPICAL MODULATED SIGNAL

FIGURE 1.2 SLOW CODE - TYPE 'A'



	RATE	TIME FRAME	D-PERIOD	A-WIDTH OF REF. MARKER	B-WIDTH OF BINARY ONE	C-WIDTH OF BINARY ZERO	E-WIDTH OF INDEX MARKER	NO. OF PULSES IN TIME FRAME
1	50 pps	1 Sec.	20 ms	20 ms	10 ms	4 ms	4 ms	50
2	10 pps	5 Secs.	100 ms	100 ms	50 ms	20 ms	20 ms	50
3	5 pps	10 Secs.	200 ms	200 ms	100 ms	40 ms	40 ms	50
4	1 pps	30 Secs.	1 Sec	1 Sec.	500 ms	200 ms	200 ms	30
5	1 2 pps	60 Secs	2 Secs.	2 Secs.	1 Sec.	400 ms	400 ms	30
6	1 10 pps	5 Mins.	10 Secs.	10 Secs.	5 Secs.	2 Secs.	2 Secs.	30
7	1 20 pps	10 Mins.	20 Secs.	20 Secs.	10 Secs.	4 Secs.	4 Secs.	30
8	1 ppm	30 Mins.	1 Min.	1 Min.	30 Secs.	12 Secs.	12 Secs.	30
9	1 2 ppm	60 Mins.	2 Mins.	2 Mins.	1 Min.	24 Secs.	24 Secs.	30

FIGURE 1.3 SLOW CODE - TYPE 'B'



Pulse Rate	Time Frame	D-Period	A-Width	B-Width	C-Width	E-Width	Number of Pulses in Time Frame
1. 50	1 SEC	20 ms	20 ms	10 ms	4 ms	4 ms	50
2. 10	5 SEC	100 ms	100 ms	50 ms	20 ms	20 ms	50
3. 5	10 SEC	200 ms	200 ms	100 ms	40 ms	40 ms	50
4. 2	30 SEC	1/2 SEC	1/2 SEC	250 ms	100 ms	100 ms	60
5 1	60 SEC	1 SEC	1 SEC	1/2 SEC	200 ms	200 ms	60
6 1/2	5 MIN	5 SEC	5 SEC	2-1/2 SEC	1 SEC	1 SEC	60
7 1/10	10 MIN	10 SEC	10 SEC	5 SEC	2 SEC	2 SEC	60
8. 2 ppm	30 MIN	30 SEC	30 SEC	10 SEC	6 SEC	6 SEC	60
9 1 ppm	60 MIN	60 SEC	60 SEC	30 SEC	12 SEC	12 SEC	60

FIGURE 1.4 AMR TIME CODE FORMATS

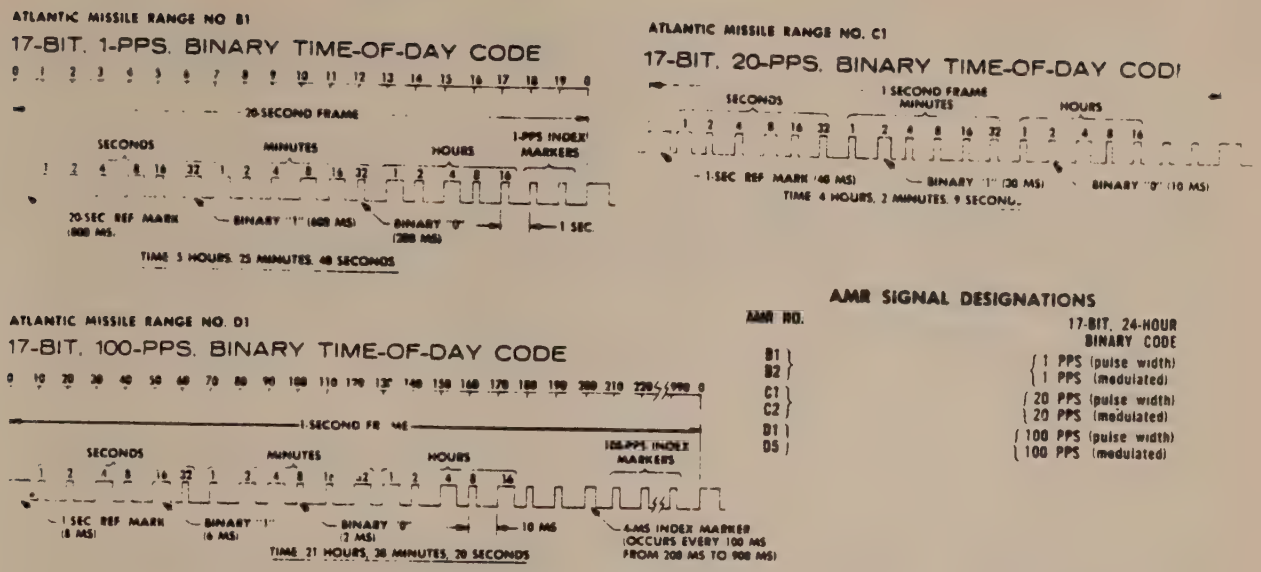
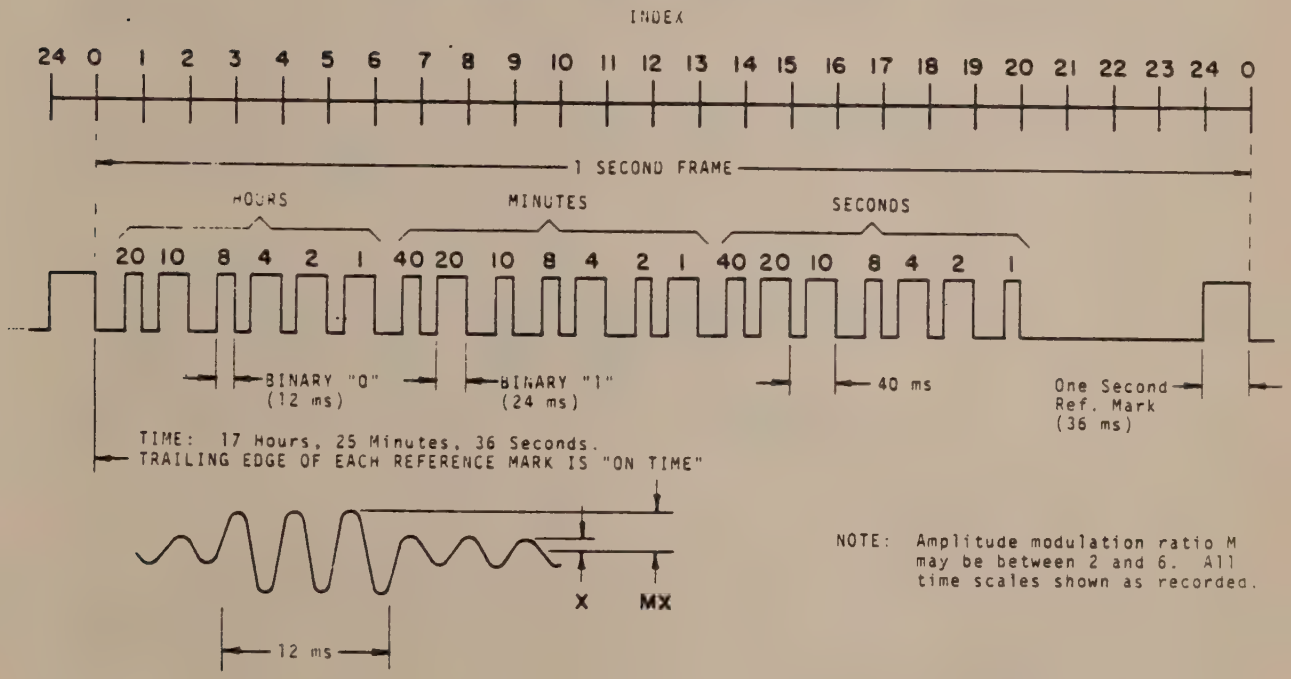

ATLANTIC MISSILE RANGE NO. B1
17-BIT, 1-PPS, BINARY TIME-OF-DAY CODE
20-SECOND FRAME
SECONDS
MINUTES
HOURS
1-PPS INDEX MARKERS
20-SEC REF MARK (800 MS)
BINARY "1" (600 MS)
BINARY "0" (200 MS)
1 SEC
TIME 5 HOURS, 25 MINUTES, 40 SECONDS
ATLANTIC MISSILE RANGE NO. C1
17-BIT, 20-PPS, BINARY TIME-OF-DAY CODE
1 SECOND FRAME
SECONDS
MINUTES
HOURS
1-SEC REF MARK (40 MS)
BINARY "1" (30 MS)
BINARY "0" (10 MS)
TIME 4 HOURS, 2 MINUTES, 9 SECONDS
ATLANTIC MISSILE RANGE NO. D1
17-BIT, 100-PPS, BINARY TIME-OF-DAY CODE
1-SECOND FRAME
SECONDS
MINUTES
HOURS
100-PPS INDEX MARKERS
1 SEC REF MARK (8 MS)
BINARY "1" (6 MS)
BINARY "0" (2 MS)
10 MS
6-MS INDEX MARKER (OCCURS EVERY 100 MS FROM 200 MS TO 900 MS)
TIME 21 HOURS, 38 MINUTES, 20 SECONDS
AMR SIGNAL DESIGNATIONS
AMR NO.
17-BIT, 24-HOUR BINARY CODE
B1, B2: 1 PPS (pulse width), 1 PPS (modulated)
C1, C2: 20 PPS (pulse width), 20 PPS (modulated)
D1, D5: 100 PPS (pulse width), 100 PPS (modulated)

FIGURE 1.5 XR3 TIME CODE FORMAT


INDEX
24 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 0
1 SECOND FRAME
HOURS
MINUTES
SECONDS
20 10 8 4 2 1 40 20 10 8 4 2 1 40 20 10 8 4 2 1
BINARY "0" (12 ms)
BINARY "1" (24 ms)
40 ms
One Second Ref. Mark (36 ms)
TIME: 17 Hours, 25 Minutes, 36 Seconds.
TRAILING EDGE OF EACH REFERENCE MARK IS "ON TIME"
X
MX
12 ms

NOTE: Amplitude modulation ratio M may be between 2 and 6. All time scales shown as recorded.

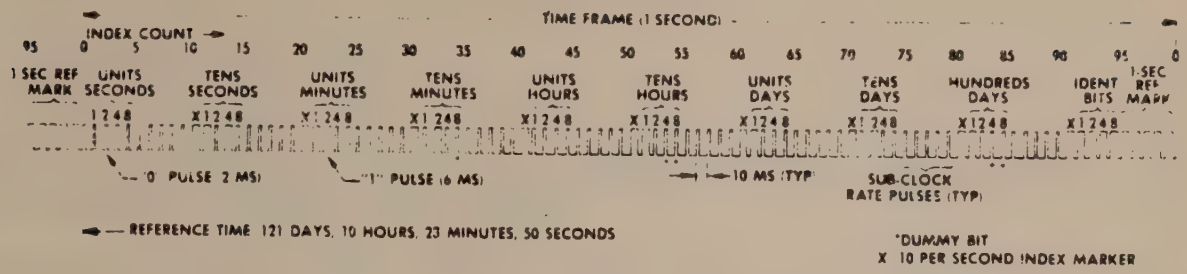
TYPICAL MODULATED CODE ELEMENT "ZERO" (250 Hz Carrier)

For 1 kHz carrier large amplitude cycles number 12, 24, and 36

FIGURE 1.6 NASA TIME CODE FORMATS

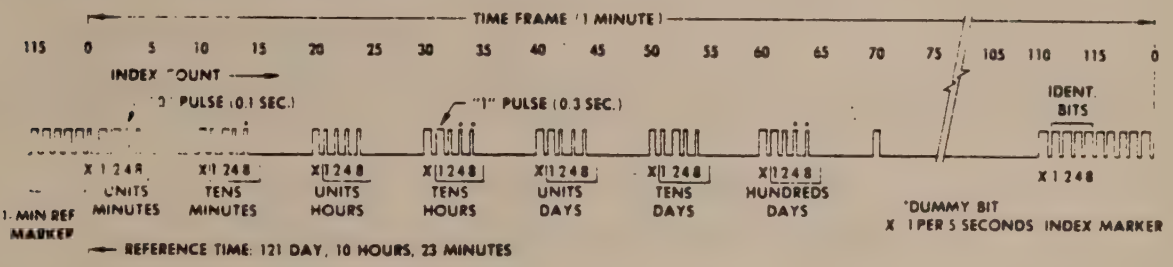
36-BIT, 100-PPS CODE (1000-CPS CARRIER)

SHOWING SUB-CLOCK RATE PULSES


TIME FRAME (1 SECOND)
INDEX COUNT
95 0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 80 85 90 95 0
1 SEC REF MARK
UNITS SECONDS
TENS SECONDS
UNITS MINUTES
TENS MINUTES
UNITS HOURS
TENS HOURS
UNITS DAYS
TENS DAYS
HUNDREDS DAYS
IDENT BITS
1 SEC REF MARK
X 1 2 4 8
"0" PULSE (2 MS)
"1" PULSE (6 MS)
10 MS (TYP)
SUB-CLOCK RATE PULSES (TYP)
REFERENCE TIME: 121 DAYS, 10 HOURS, 23 MINUTES, 50 SECONDS
*DUMMY BIT
X 10 PER SECOND INDEX MARKER

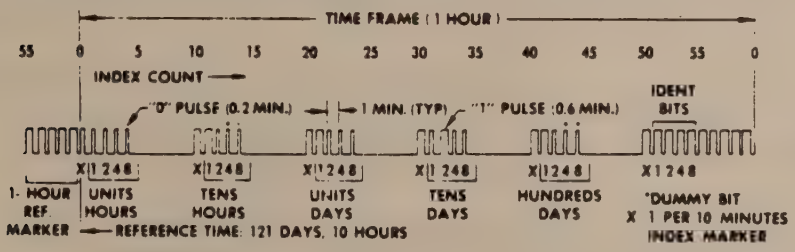
28-BIT, 2-PPS CODE (100-CPS CARRIER)

SUB CLOCK RATE PULSES INHIBITED

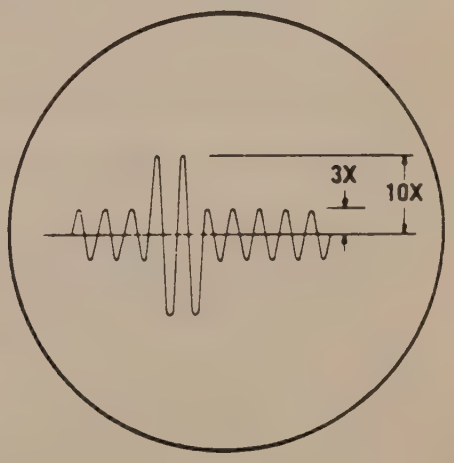

TIME FRAME (1 MINUTE)
115 0 5 10 15 20 25 30 35 40 45 50 55 60 65 70 75 105 110 115 0
INDEX COUNT
"0" PULSE (0.1 SEC.)
"1" PULSE (0.3 SEC.)
IDENT. BITS
X 1 2 4 8
1-MIN REF MARKER
UNITS MINUTES
TENS MINUTES
UNITS HOURS
TENS HOURS
UNITS DAYS
TENS DAYS
HUNDREDS DAYS
*DUMMY BIT
X 1 PER 5 SECONDS INDEX MARKER
REFERENCE TIME: 121 DAY, 10 HOURS, 23 MINUTES

20-BIT, 1-PPM CODE (100-CPS CARRIER)

SUB-CLOCK RATE PULSES INHIBITED



Insertion of sub-clock rate pulses is controlled for each format by individual control switches.



TYPICAL MODULATED SIGNAL

CHAPTER TWO
INSTALLATION

2.1 INITIAL INSPECTION

As soon as the instrument is received, verify that it is intact and as ordered. Inspect it for damage. If any shipping damage is found refer to the warranty at the front of this manual and to Section 2.2 for re-packaging and shipping instructions.

As soon as possible, the instrument should be installed and given a thorough electrical inspection. Should the instrument fail to operate properly or fail to meet the listed specifications, immediately contact your Systron-Donner representative.

2.2 STORAGE AND RESHIPMENT

Environmental conditions during storage and shipment should be limited as follows:

Maximum Temperature: 185°F (85°C)

Minimum Temperature: -69°F (-55°C)

To protect your instrument during shipment or storage, use the best packaging methods available. Your Systron-Donner field office can provide materials similar to those used for original factory packaging. Contract packaging companies can provide dependable packaging on short notice.

General packaging instructions:

1) Wrap the instrument in heavy paper or plastic before placing it in the shipping container.

2) If possible, use the original container designed for the instrument. Otherwise, use a strong carton (350 lb. sq in. bursting strength) or wooden box to house the instrument.

3) Use plenty of packaging material around all sides of the instrument and protect the front panel with cardboard strips.

4) Seal the package with strong tape or metal bands. Mark the package with "DELICATE INSTRUMENT".

5) Refer to the warranty at the front of this manual and check with your Systron-Donner field office for shipping instructions. All correspondence should refer to the instrument by its model number and full serial number.

2.3 POWER AND COOLING REQUIREMENTS

The Model 8132, unless otherwise specified, is supplied to operate from a 115 V ± 10%, 48 to 62 Hz source.

To adapt the Model 8132 for 230 V operation, push the rear panel 115/230 V selector switch, S101, to the "230" position and change Fuse, F1, from 2 A slow-blow to 1 A slow-blow.

2.4 INITIAL ADJUSTMENT

To apply primary power to the Model 8132, it is only necessary to turn the READER MODE switch to PWR OFF, install the power cord (supplied), and turn the switch to READ 0E. Introduce the appropriate code via connector J8. The unit should translate and display the time information contained in the code, provided the input code is within specifications. No adjustment of the AGC (AGC/Cycle Detector card A10) should be necessary.

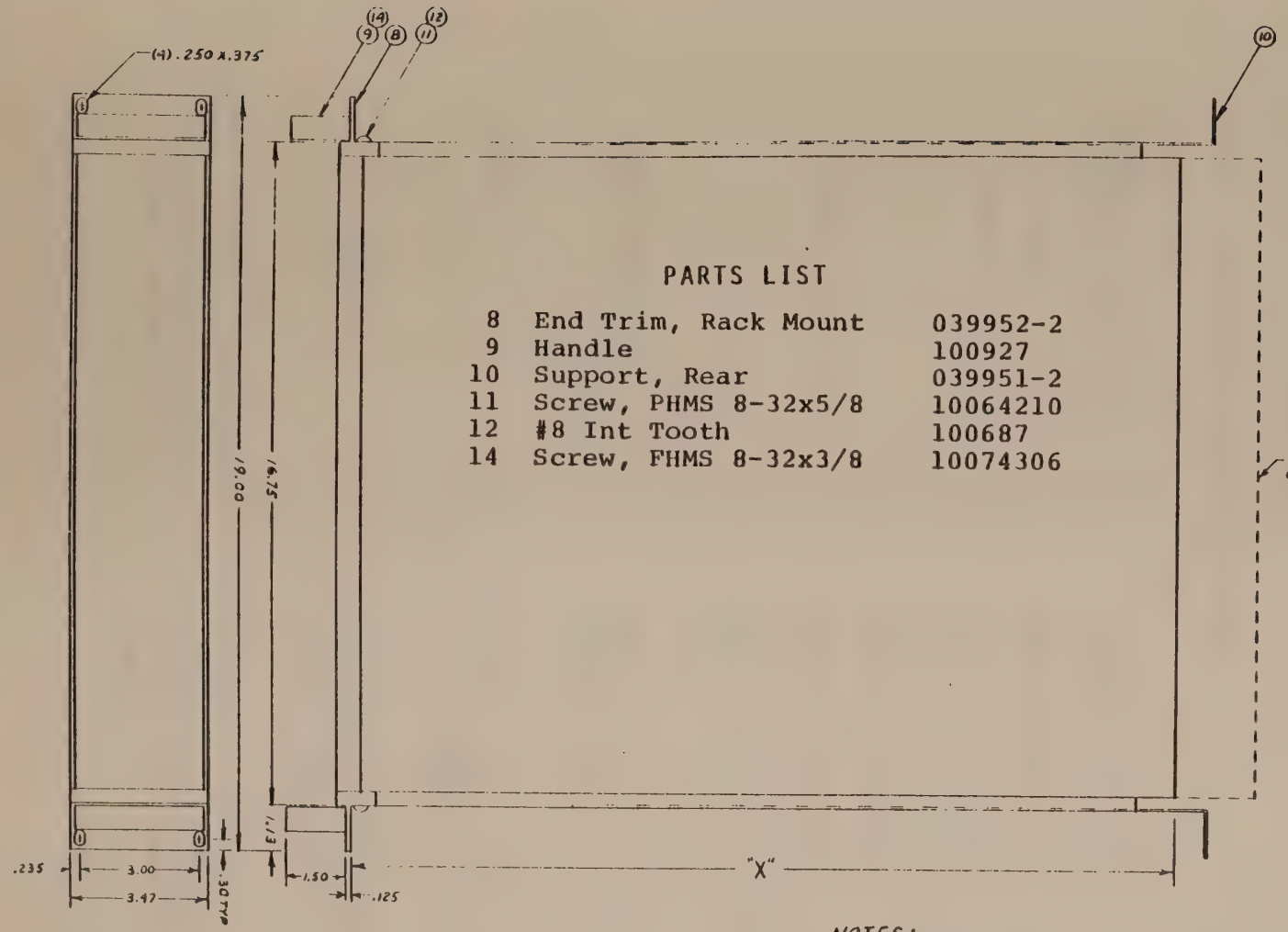
2.5 INSTALLATION

The Model 8132 is normally supplied with hardware for rack-mount installation as shown in Figure 2.1.

For convenience, the unit has been drilled for 20" Jonathan 120 QD series slides. When slides are used, the rear support brackets (Item 10) are removed.

NOTE

Under no condition should air flow through the outlet hole in the rear of the unit be obstructed.



TABULATION		
P/L #	"X"	INSTR. DEPTH
39986-1	8.75	9.12
39986-2	10.75	11.12
39986-3	12.75	13.12
39986-4	14.75	15.12
39986-5	16.75	17.12
39986-6	18.75	19.12
39986-7	20.75	21.12

NOTES:

1. INSTR. ARE DRILLED TO ACCEPT 20" JONATHAN 120 QD SERIES SLIDES
2. ITEM 10 DELETED WHEN SHIPPED W/SLIDES

FIGURE 2.1 3½" FULL RACK ASSEMBLY #039986-4-5 REV A

CHAPTER THREE
OPERATION

3.1 GENERAL

The Model 8132 is ready to operate immediately after turning on the power. Preliminary adjustments or calibration are not normally required. It is advisable that the following description on use of the instrument controls and indicators be read before operating the unit.

3.2 CONTROLS, INDICATORS AND CONNECTORS

3.2.1 Front Panel

1) MODE Selector: (Rotary Switch S30) — Controls main power and selects mode of operation.

   PWR OFF: — Removes power to the unit.

   READ OE: — Places the unit in a Read Mode condition which allows time information to be stripped from the input code and loaded into the display register.

   READ 3E: — Places the unit in a Read Mode condition such that transfer of time information into the display register is inhibited for up to three frames if an error is detected in forward.

2) TAPE DIRECTION: (Toggle Switch, S35) — NORMal position conditions unit to read a forward code. The REVerse position permits a reverse code to be read.

3) DISPLAY: — A 6-digit, in-line, planar readout which indicates TOD in hours, minutes and seconds. Days/ID option adds 3-digits.

4) TAPE ERROR: (LED, DSI) — Indicates a discrepancy between the input code and the contents of the display register when in Error Bypass Mode.

3.2.2 Rear Panel

1) BCD OUT/SEARCH CONTROL: (50-pin connector, J3) — BCD Output of display register contents plus search control signals.

2)	PULSE RATE: (14-pin connector, J4)	Pulse rate and control lines.
3)	CODE IN: (BNC connector, J8)	Modulated Code input to Reader.
4)	AC POWER: (AC connector, J101)	Mates with ac line cord.
5)	115/230 V Power Select: (Slide switch, S101)	Adapts power transformer for 115 or 230 volt operation.
6)	BCD MS, Optional: (14-pin connector, J6)	BCD milliseconds outputs.
7)	Remote, Optional: (36-pin connector, J7)	Reserved for options.
8)	SLOW CODE, Optional: (BNC connector, J11)	Slow time code output.
9)	365-366-ID, Optional: (Slide switch, S33)	Leap Year/ID selector switch (part of Days/ID option).
10)	Auxiliary, Optional: (50-pin connector, J5)	Reserved for options.

CHAPTER FOUR

MAINTENANCE AND CALIBRATION

4.1 FACTORY SERVICE

When the instrument requires service, the nearest Systron-Donner representative should be contacted. He can provide field service or arrange for factory returns, when necessary. Address all inquiries on operation or applications to your nearest sales representative; or Sales Manager:

SYSTRON-DONNER CORPORATION
CONCORD INSTRUMENT DIVISION
2727 Systron Drive
Concord, California 94518
Phone: (415) 676-5000
TWX: 910-481-9479
Cable: SYSTRON DONNER

Specify both model and complete serial number in all correspondence.

4.2 ROUTINE MAINTENANCE

A regular program for maintenance and inspection every five to six months is recommended for this unit. As part of these regular procedures, the instrument should be checked in the following manner:

1) Disconnect ac power and remove the top and bottom covers.

2) Make a thorough visual inspection of all wiring and cables. Check for frayed, loose, or burned wires.

3) Check the physical integrity of all components. Look for burned or cracked components, loose solder connections, leakage of insulation compounds, and general physical damage. When a printed-circuit board contains integrated-circuit packages, ensure that all packages are firmly mounted. Never unnecessarily remove and replace a package.

4) Check all front panel switches and controls for loose or broken terminals, loose or sticking shafts, etc.

5) If the internal panel surfaces and components have an excessive amount of dust deposited on them, use a soft brush and low-pressure stream of air to remove the foreign material.

CAUTION

Do not clean P.C. boards or small internal components with a stiff brush or solvents, since damage to the circuits may result. A high-powered vacuum cleaner device should not be used on small internal components.

6) Wipe the external surfaces of the instrument with a soft, damp cloth to remove dirt, fingerprints, and other foreign materials.

7) Replace the top and bottom covers and reconnect ac power. Perform the Operational Test and Calibration Procedure (Section 4.4). If performance does not match or exceed the specifications listed in Chapter 1 of this manual, corrective maintenance is in order.

4.3 PRINTED-CIRCUIT BOARD REPAIR

When replacing integrated circuits or other electronic components soldered to printed-circuit boards, the procedures indicated below must be followed or damage to the board may result:

1) Determine by troubleshooting techniques, which integrated circuit or discrete component(s) has failed.

2) Remove the defective component(s) from the board by cutting the pins or leads with a small diagonal clipping tool. (Always remove and replace the entire component).

3) Apply heat (40-50-W soldering iron) sparingly to each of the cut pins or leads and remove from the board; clean the hole(s) with a toothpick or solder suction tool.

4) Form the tinned leads of the replacement part and insert in the printed-circuit holes; solder, then trim leads to extend 1/16 inch beyond the back surface of the board. (Use only 63-37 solder with maximum 1/16 inch diameter).

CAUTION

Always trim semiconductor leads only after soldered installation is complete. This procedure greatly lessens the possibility of component failure due to shock-wave damage caused by the trimming tool.

5) When soldering semiconductor devices and all small components, be sure to use a heat sink tool or long-nosed plier connected to the component lead(s) while each is being soldered. Allow the solder connection to cool before removing the heat sink.

6) Clean all dirt and solder-flux from the printed circuit traces by liberal application of isopropyl alcohol or freon-type solvents.

4.4 OPERATIONAL TEST AND CALIBRATION PROCEDURE

In the event of an equipment malfunction the following circuit description and adjustment procedure, if followed in the listed sequence, will allow the service engineer to isolate the trouble to a particular circuit card or subsection.

When the trouble is isolated, the functional description in Chapter 5 and option information in Chapter 6 will facilitate repair.

WARNING

Dangerous high voltages are present in the power supply of this equipment. Use caution at all times when the protective covers are removed.

4.4.1 Recommended Test Equipment

The following test equipment or equivalent is recommended for use in servicing the Model 8132.

TABLE 4.1 TEST EQUIPMENT FOR MODEL 8132

Model	Manufacturer	Minimum Specifications
422	Tektronix, Inc.	Oscilloscope, 15 MHz bandwidth, triggered sweeps from 0.1 microseconds/cm to 5 sec/cm. Vertical sensitivity from .05 volts/cm to 20 volts/ cm.
6012	Tektronix, Inc.	Probe, 10:1 attenuation ratio, 17 pF capacitance.
7003	Systron-Donner Corp.	DMM 10 MΩ input impedance, ±0.1% accuracy.
200AB	Hewlett Packard	Audio Oscillator, 20 Hz to 40 kHz coverage.
6250	Systron-Donner Corp.	Frequency Counter, 0 Hz to 50 MHz, 3 parts/10^7 per week.

In addition to the equipment listed above, a suitable source of time code input signals with known characteristics is required. This may be a Time Code Generator or a prerecorded tape and tape playback equipment.

4.4.2 Power Supply (Dwg. #41810-7-9)

The voltage checks listed below will ensure the correct operation of the power supply, assuming a normal line voltage of 115 V ac.

The voltages listed below are unregulated and nonadjustable. The test points are available on the unit PC edge connector, P103.

1) Ensure the presence of +210 V dc ±25% at pins V,18 (fuse F2).

2) Ensure the presence of +21 V dc ±20% at pins S,15 (fuse F3).

3) Ensure the presence of +9 V dc ±20% at pins Y,21.

4) Ensure the presence of -9 V dc ±20% at pin 2.

5) Ensure the presence of -21 V dc ±20% at pin 4.

4.4.3 Power Supply Regulator (Dwg. #41810-7-9)

Adjust the following voltages on the Power Supply Regulator board. The test points are located on the power supply PC board (Dwg. #41804-4-9) near the adjustment potentiometers.

TABLE 4.2

POWER SUPPLY REGULATOR VOLTAGE ADJUSTMENTS

Voltage	Adjust	Test Point
+15 V dc ±0.5%	R5	Blue
-15 V dc ±0.5%	R5	Violet
+5 V dc ±0.5%	R19	Red
-5 V dc ±0.5%	R19	Green

If the Power Supply Regulator is operating normally, and the unregulated voltages are correct, the above voltages will be obtained with little difficulty. If they do not adjust properly, or fail to maintain regulation, corrective maintenance is in order.

4.4.4 AGC & Cycle Detector (Dwg #21569-7-1)

1) Preliminary Set-Up

   a) Connect a time code source to "CODE IN" BNC connector on rear panel of the unit (signal level approximately 3 volts peak-to-peak).

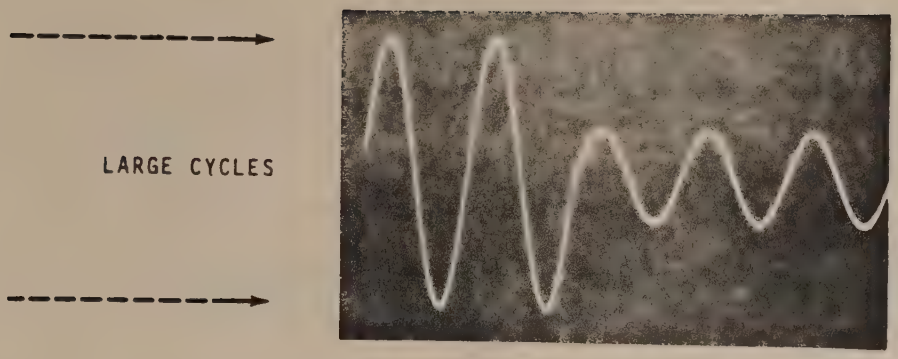


FIGURE 4.1 AGC LEVEL ADJUSTMENT

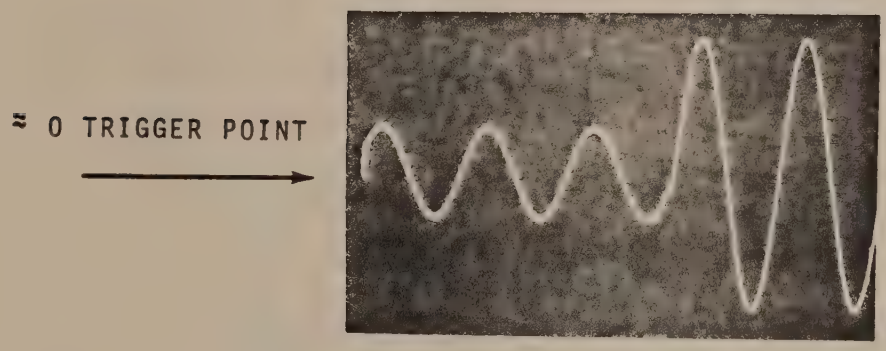


FIGURE 4.2 CYCLE DETECTOR ADJUSTMENT

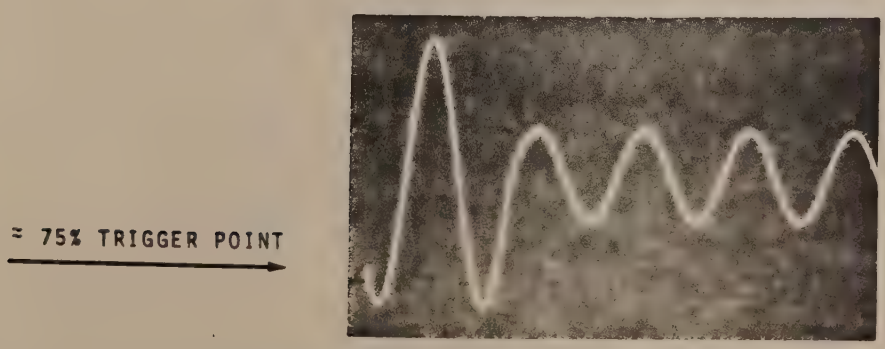


FIGURE 4.3 LOWER LARGE CYCLE ADJUSTMENT

b) Place unit in either Read Mode.

CAUTION

Do not place AGC & Cycle Detector on extender board when performing these adjustments.

2) AGC Level

a) Monitor "TRIG" test point with oscilloscope.

(1) Adjust "AGC" potentiometer R4 so that the large cycles (see Figure 4.1 AGC Level Adjustment) are 2.75 volts peak-to-peak ±5%.

(2) Reduce level of incoming time code signal to approximately 1 volt peak-to-peak.

Allow approximately 5 seconds for AGC to recover. Signal at "TRIG" test point should remain the same amplitude as adjusted in Step (1).

3) Cycle Detector

a) Monitor "TRIG" test point with oscilloscope

(1) EC, Each Cycle,Adjustment.

Set oscilloscope to trigger positive (+), external trigger. Connect external trigger input of oscilloscope to "EC" test point.

Turn R25 "EC" Adjust, full clockwise. Turn in the CCW direction until each cycle is triggering approximately 30% up on the positive slope of the small cycles (see Figure 4.2, Cycle Detector Adjustment).

(2) LLC, Lower Large Cycles Adjustment

Set oscilloscope to trigger negative (-), external trigger. Connect external trigger input of oscilloscope to $\overline{\text{LLC}}$ test point.

Turn R34 "LLC" Adjust, full clockwise. Turn in the CCW direction until the lower large cycles are triggering approximately 75% of the way down on the negative slope of the lower large cycles (see Figure 4.3 Lower Large Cycle Adjustment).

4.4.5 Reverse Operation

With the Model 8132 in either Read Mode, check that it will read in the forward and reverse directions as follows: Place the TAPE DIRECTION

switch in the NORMal position for a foward code and in the REVerse position for a reverse code direction.

4.4.6 Sensitivity

If possible, vary the input code voltage within the limits specified in Chapter One and observe that the unit reads the code normally in both forward and reverse directions.

4.4.7 Frequency Response

If possible, vary the rate of the input code within the limits of carrier frequency specified in Chapter One and observe that the unit reads the code normally in both forward and reverse directions.

4.4.8 Error Bypass (Dwg. #7-05153802)

1) Using a separate time code generator in a HOLD mode, produce a continuous time code which is not updated. Connect this signal to the "CODE IN" BNC connector on the rear panel of the Model 8132.

2) Place the Model 8132 MODE selector switch in READ 3E (Error Bypass) position. Observe that the units-of-seconds updates 3 numbers and returns to the number displayed on the test unit generator.

3) Place the test generator MODE switch in GENerate position. The translator should update in the normal manner.

4.4.9 General Checkout

No additional adjustments are required in the instrument. To facilitate tracing possible malfunctions, determine if each plug-in card is performing in accordance with the circuit description provided in other sections of this manual. It is advisable to determine proper operation of the boards in the order of decreasing signal repetition rate.

CHAPTER FIVE
FUNCTIONAL DESCRIPTION

5.1 GENERAL

The Model 8132 is a Time Code Reader capable of translating a modulated time code in either the forward or reverse direction. Schematics and specific card assembly descriptions relating to the basic unit are provided at the end of the chapter. Standard options, when included, are described in Chapter 6. Special modifications, if any, are presented in Chapter 7.

5.1.1 Reference Designations

Reference designations are confined to the assembly under discussion since it is usually clear from the contest which assembly is involved.

When citing a subelement of a multielement integrated circuit, the reference designation of the integrated circuit is given, followed by the number of the output terminal.

When citing flip-flops formed from two gates on the same chip, the reference designation of the chip is given followed by the two output pin numbers. The reference designations used in the Model 8132 are listed in Table 5.1.

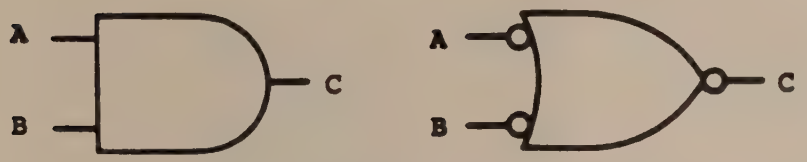
TABLE 5.1
REFERENCE DESIGNATIONS

A or U	Integrated Circuit
C	Capacitor
CR	Diode
DS	Lamp
F	Fuse
FL or Z	Filter
J	Jack
L	Inductor
P	Plug
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
W	Jumper
X	Socket

5.1.2 Logic Functions

The Logic symbols and functions used in the Model 8132 are described as follows:

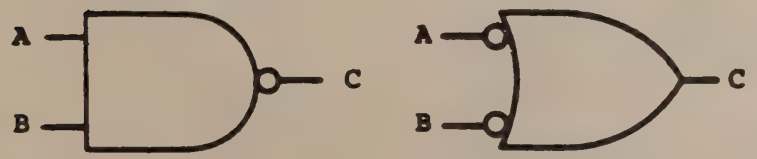
AND Gate **INVERTED NOR Gate**



A	B	C
0	0	0
0	1	0
1	0	0
1	1	1

The AND Gate and INVERTED NOR Gate have the same truth table.

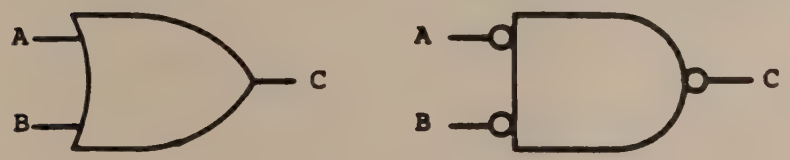
NAND Gate **INVERTED OR Gate**



A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

The NAND Gate and INVERTED OR Gate have the same truth table.

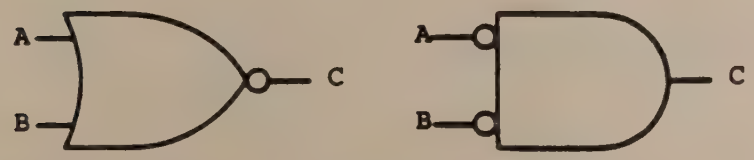
OR Gate **INVERTED NAND Gate**



A	B	C
0	0	0
0	1	1
1	0	1
1	1	1

The OR Gate and INVERTED NAND Gate have the same truth table.

NOR Gate **INVERTED AND Gate**



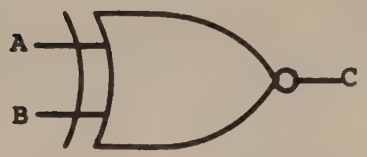
A	B	C
0	0	1
0	1	0
1	0	0
1	1	0

The NOR Gate and INVERTED AND Gate have the same truth table.

EXCLUSIVE OR

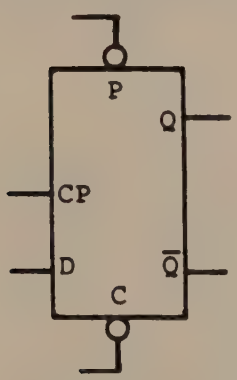
A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

EXCLUSIVE NOR



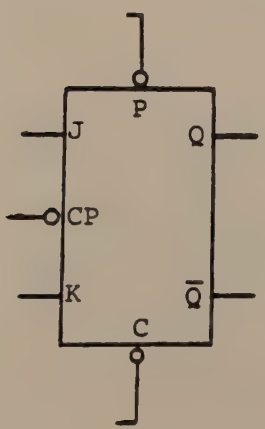
A	B	C
0	0	1
0	1	0
1	0	0
1	1	1

D-TYPE Flip-Flop



1) Q assumes the state of the D input on the positive transition of the clock (CP) input.
2) The D input is locked out when the clock input is positive.
3) P and C override all other inputs.
4) If $\overline{P}$ and $\overline{C}$ are both at Logic 0, the Q and $\overline{Q}$ outputs are both at Logic 1.
5) At a set condition, Q is Logic 1. At a clear condition, Q is a Logic 0.

JK-TYPE Flip-Flop



1) When J and K are both at a Logic 0, no change will occur.
2) When K is a Logic 1, Q will be a Logic 0.
3) When J is a Logic 1, Q will be a Logic 1.
4) When J and K are both at a Logic 1, the flip-flop will change state.
5) $\overline{P}$ and $\overline{C}$ override all other inputs.
6) CP is the clock input.

In some configurations it is possible to perform the AND and OR functions simply by tying the outputs of certain gates together.

These functions are called DOT AND and DOT OR functions. The nature of the signals fed to the "DOT" determines whether the function is AND or OR. When several "DOTS" are present on a single line the AND or OR symbol is used only once.

DOT AND

DOT OR

5.2 Function

The Model 8132 Time Code Reader accepts a serial modulated IRIG B time code input. It strips time informations from the code in bytes and loads it into the TOD Accumulator. The time in the accumulator is displayed. It is also available for output in parallel through buffers on card A16. Circuits are included to maintain the accumulator on time in forward mode and to regenerate a serial code for comparison with the input in the Error Bypass mode of operation. (Days/ID and/or the translation of other time codes may be included as options). The basic Reader is shown in block form on Drawing #06103402.

5.2.1 AGC/Cycle Detector (Dwg. #021569-7-1)

Referring to the block diagram, the modulated input code is fed through connector J8 to AGC/Cycle Detector card (A10). The AGC circuit on this card establishes a standard level signal from which two signals are derived. The first of these is the EC (Each Cycle) signal which is a square wave at the carrier frequency. The second is the $\overline{\text{LLC}}$ (Lower Large Cycle) signal. Both signals are fed to Reader Logic card (A12). The EC signal is also fed through selection gates on Preset and Error Bypass card (A11), emerging as the $\overline{\text{Z-RATE}}$ signal to the Minor Couter card (A9) and Code Generator card (A17).

5.2.2 Reader Logic (Dwg. #021588-7-3)

The Reader Logic card (A12) contains a 9-bit shift register which accumulates time information stripped from the input code. This register is cleared and a ONE entered by the double-mark at the beginning of the time frame. This is followed by each subsequent bit as it is detected. When the initial ONE is in the 9 position, the contents of the shift register are transferred into the seconds section of the TOD Accumulator card (A15). The next index mark clears the register and enters a ONE followed by minutes information. These bits are transferred to the minutes section of the accumulator. In like manner, hours (and days) bits are detected and transferred. (Days are loaded into Days Accumulator A18 when the Days/ID Option is included.)

5.2.3 Minor Counter (Dwg. #021632-7-2)

Once the Time Code Reader is synchronized with the input code (in forward), the TOD Accumulator card (A15) plus A18 with Option E13, already contains the current information being transferred in. This is accomplished by the Minor Counter card (A9) which derives a 1 pps, on-time update pulse from the Z-RATE signal. This signal updates the accumulator on-time at the beginning of each frame.

The Minor Counter card (A9) is a three-decade divider which divides the 1 KHz (Z-RATE) input down to 1 pps to drive the TOD Accumulator (card A15) and provide a sync signal for Code Generator card (A17). A separate set of buffers are provided for parallel BCD milliseconds outputs for Option E14 (Millisecond Outputs). Pulse rates (1 Kpps, 100 pps, 10 pps and 1 pps) are provided at connector J4.

5.2.4 TOD Accumulator (Dwg. #021543-7-3)

The TOD Accumulator card (A15) accepts the 1 pps (8×10^{-1}) output from the Minor Counter card (A9) and divides it into units and tens-of-seconds, minutes and hours. The decade and scale-of-six dividers which accomplish this can be parallel preset, as well as provide parallel BCD outputs. This permits the time stripped from the input code by the Reader Logic card (A12) to be loaded. The parallel BCD outputs feed: 1. The Display Assembly (A102); 2. the Code Generator (A17); and, 3. Buffer (A16) to provide TOD outputs. The 1 ppd output is fed to Days Accumulator (A18) as parts of Option E13, Days/ID. See Chapter Six.

5.2.5 Code Generator (Dwg. #021554-7-1)

The Code Generator card (A17) accepts the parallel TOD inputs and developes a serial level shift code complete with index and frame markers. Days/ID are replaced by zeros in the code in the absence of Option E13. The level shift code is fed to Preset and Error Bypass card (A11).

5.2.6 Preset and Error Bypass (Dwg. #7-05153802)

The serial level shift code from the Code Generator card (A17), containing the time from the accumulator, is compared with the incoming code in circuits on Preset and Error Bypass card (A11). When operating in the Error Bypass mode, this circuitry inhibits the transfer of up to three consecutive input code frames if a discrepancy is detected.

5.2.7 FWD-REV Control

The Time Code Reader is capable of reading the input code in the reverse direction as well as forward except that Error Bypass does not function in reverse. The conditions for reverse read operation are established by circuits on FWD-REV Control card (A13) in response to signals from the TAPE DIRECTION switch or the REV input through connector J3. Circuits on card (A13) invert the order in which bits are transferred to the Accumulator, suppress the 1 pps update signal and inhibit Error Bypass when reading a reverse code. In reverse, the contents of the Accumulator are no longer on-time.

5.4 CIRCUIT DESCRIPTIONS

The Circuit Descriptions contained in this Chapter are used in several Systron Donner Models. As a result, references may be made to control lines, circuits or functions which are not applicable to the Model 8132. Notables references to PRESET and GENerate circuits (although contained, in part, on some of the PC boards), are inoperative and these sections should be disregarded.

TABLE 5.2

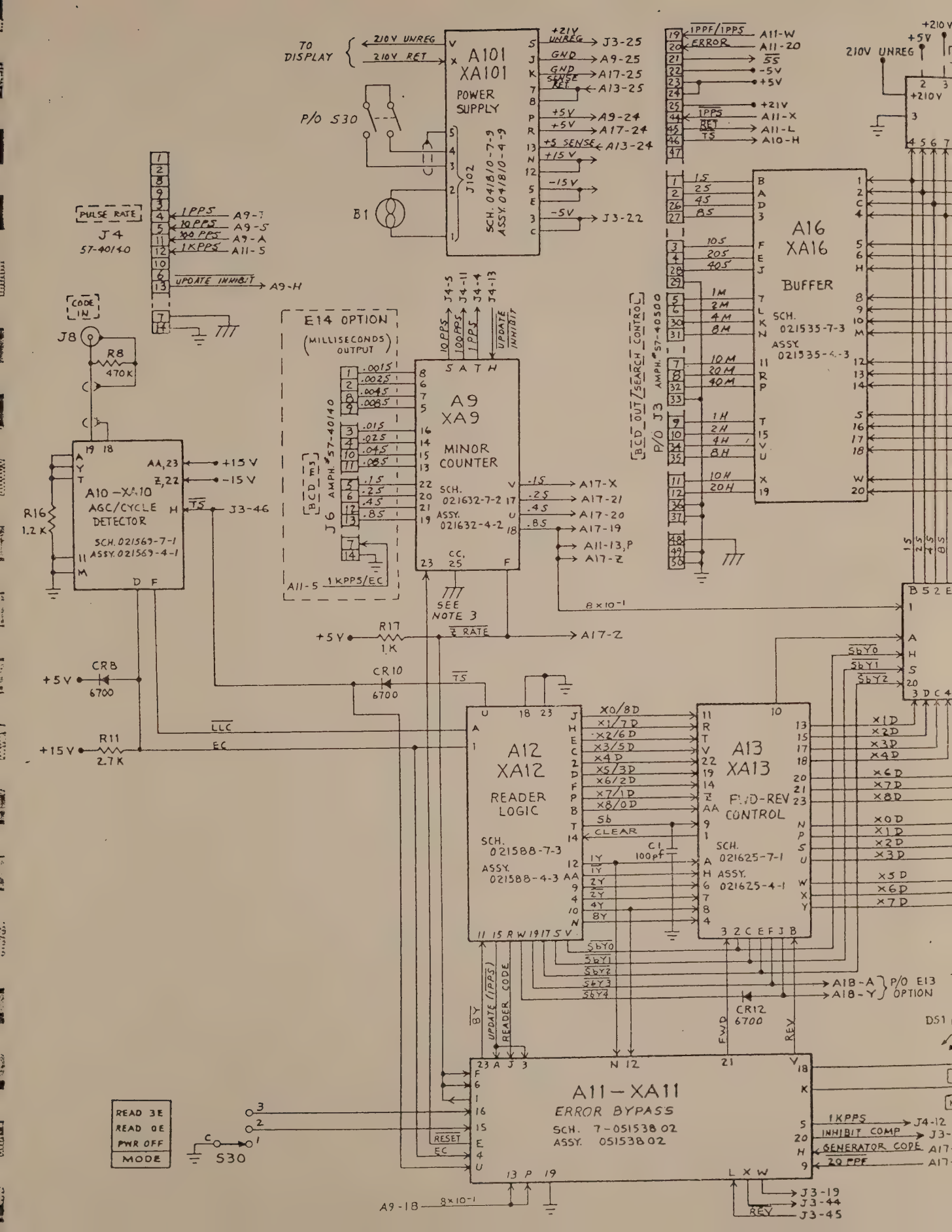
CIRCUIT DESCRIPTION INDEX INFORMATION

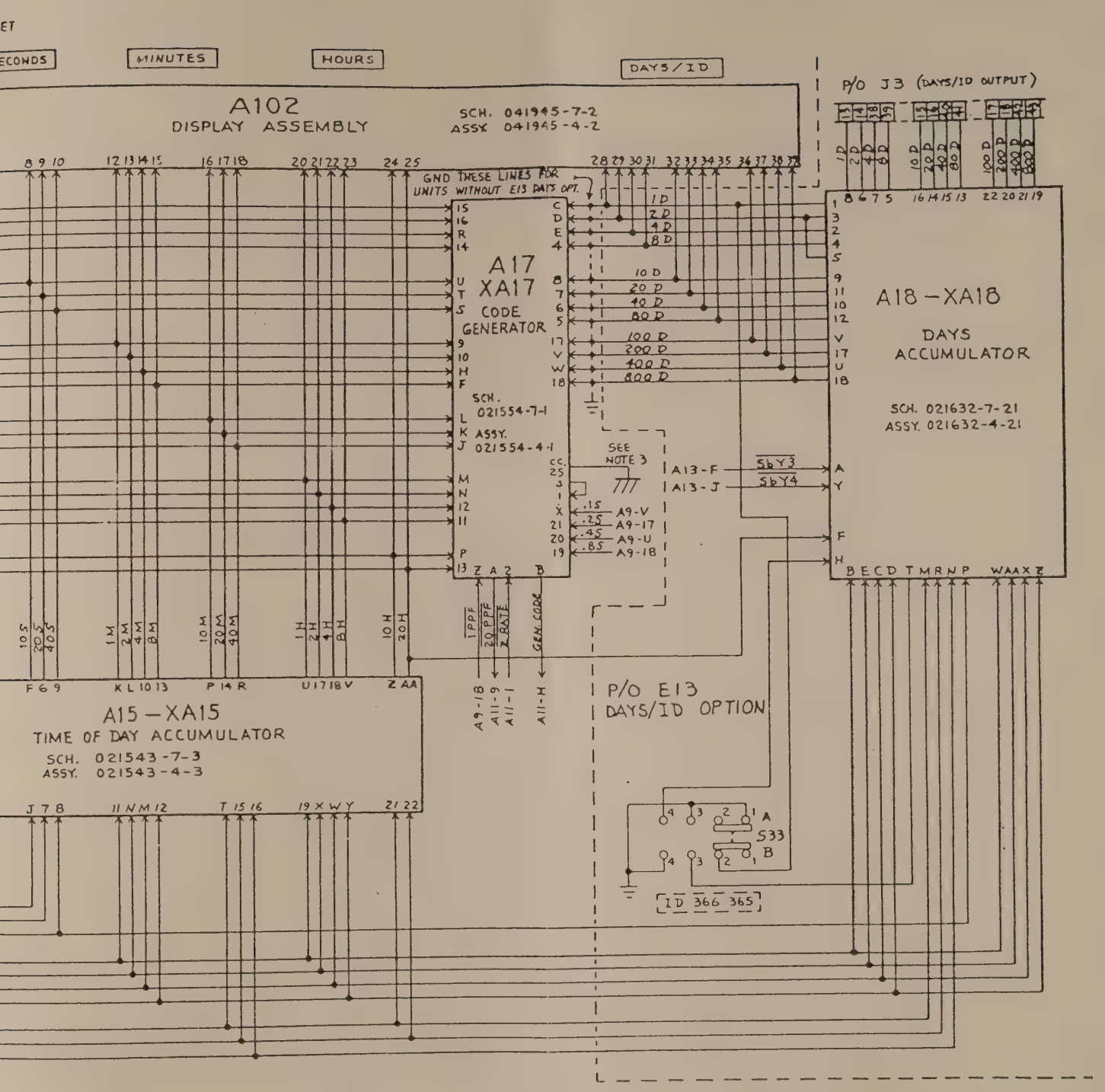
LOCATION	DESCRIPTION	SCHEMATIC #	PAGE #
A1-A8	Reserved for Options		
A9	Minor Counter	021632-7-2	5-39
A10	AGC/Cycle Detector	021569-7-1	5-25
A11	Preset and Error Bypass	05153802	5-44
A12	Reader Logic	021588-7-3	5-30
A13	FWD-REV Control	021625-7-1	5-35
A14	Reserved for Options		
A15	TOD Accumulator	021543-7-3	5-14
A16	Buffer	021535-7-3	5-10
A17	Code Generator	021554-7-1	5-18
A18	Days Accumulator (Optional)	021632-7-21	6-E13-3
A19-A27	Reserved for Options		
A101	Power Supply	041810-7-9	5-49
A102	Display Assembly	041945-7-2	5-58

All plug-in modules are designed so that the card will only fit into position if it is correctly aligned; however, caution must be exercised to ensure that a card is installed in the correct card slot. Extractor handles on all cards are numbered to facilitate correct installation.

CAUTION

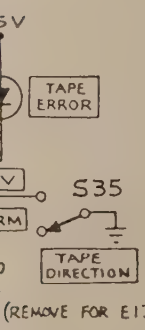
When mounting a card on the extender board, it is possible to install the card backwards which will result in serious damage.


A101
XA101
POWER SUPPLY
SCH. 04B10-7-9
ASSY. 04B10-4-9
J102
TO DISPLAY
210V UNREG
210V RET
P/O S30
B1
+21V UNREG → J3-25
GND → A9-25
GND → A17-25
SENSE RET ← A13-25
+5V → A9-24
+5V → A17-24
+5 SENSE ← A13-24
+15V
-15V
-5V → J3-22
1PPF/1PPS → A11-W
ERROR → A11-20
-5V
+5V
+21V
1PPS → A11-X
RET → A11-L
TS → A10-H
+210V
+5V
210V UNREG
PULSE RATE
J4
57-40140
1PPS → A9-7
10PPS → A9-5
100PPS → A9-A
1KPPS → A11-5
UPDATE INHIBIT → A9-H
CODE IN
J8
R8
470K
A16
XA16
BUFFER
SCH. 021535-7-3
ASSY. 021535-4-3
1S
2S
4S
8S
10S
20S
40S
1M
2M
4M
8M
10M
20M
40M
1H
2H
4H
8H
10H
20H
BCD_OUT/SEARCH_CONTROL
P/O J3 AMPH. #57-40500
E14 OPTION
(MILLISECONDS OUTPUT)
BCD
J6 AMPH. #57-40140
.0015
.0025
.0045
.0085
.015
.025
.045
.085
.15
.25
.45
.85
A11-5 1KPPS/EC
10PPS → J4-5
100PPS → J4-11
1PPS → J4-4
UPDATE INHIBIT → J4-13
A9
XA9
MINOR COUNTER
SCH. 021632-7-2
ASSY. 021632-4-2
.15 → A17-X
.25 → A17-21
.45 → A17-20
.85 → A17-19
A11-13,P
A17-Z
SEE NOTE 3
A10-XA10
AGC/CYCLE DETECTOR
SCH. 021569-7-1
ASSY. 021569-4-1
+15V
-15V
TS → J3-46
R16
1.2K
8×10⁻¹
+5V
R17
1K
Z RATE → A17-Z
CRB
6700
CR10
6700
TS
LLC
EC
+15V
R11
2.7K
A12
XA12
READER LOGIC
SCH. 021588-7-3
ASSY. 021588-4-3
X0/8D
X1/7D
X2/6D
X3/5D
X4D
X5/3D
X6/2D
X7/1D
X8/0D
5b
CLEAR
C1
100pf
1Y
2Y
4Y
8Y
A13
XA13
FWD-REV CONTROL
SCH. 021625-7-1
ASSY. 021625-4-1
X1D
X2D
X3D
X4D
X6D
X7D
X8D
X0D
X1D
X2D
X3D
X5D
X6D
X7D
5bY0
5bY1
5bY2
5bY3
5bY4
A18-A
A18-Y
P/O E13 OPTION
CR12
6700
FWD
REV
8Y
UPDATE (1PPS)
READER CODE
A11-XA11
ERROR BYPASS
SCH. 7-051538 02
ASSY. 051538 02
RESET
EC
1KPPS → J4-12
INHIBIT COMP → J3-
GENERATOR CODE → A17-
20 PPF → A17-
A9-18
8×10⁻¹
J3-19
J3-44
J3-45
REV
READ 3E
READ 0E
PWR OFF
MODE
S30



NOTES

1) +5V IS ON P.C. CARD PINS 24 & BB.
   GND IS ON P.C. CARD PINS Z5 & CC.
2) RESISTORS ARE IN OHMS, ¼W, 5%, CARBON COMPOSITION.
3) CHASSIS AND SIGNAL GROUNDS MAY BE SEPARATED BY REMOVING GND LUGS AT A9 & A17.



TIME CODE READER BLOCK DIAGRAM #06103402 REV B

PARTS LIST
FINAL ASSEMBLY #06103402

REFERENCE	DESCRIPTION	SD PART NO.
	SHIPPING ASSEMBLY REV B	#06103402
	Assembly, Test	06115502
	Trim, Front Panel	041997-1-1
	Trim, Side	039859-5
	Trim, End Rack Mount	03995202
	Window	051001-1-1
	Cover, Mounting Bracket	039857
	Cover, Top	03376005
	Cover, Bottom	03376105
	Support, Rear	03995102
	Handle	100927
P3	Connector, 50 Pin	101157
P4	Connector, 14 Pin	101181
P101	Line Cord	102407
	Foil Cal	037112
	TEST ASSEMBLY REV B	#06115502
	Assembly, Front Panel	06115301
	Assembly, Rear Panel	06115401
A101	Power Supply Assembly	041810-4-9
	Schematic	7-06103402
A9	Assembly, Minor Counter	021632-4-2
A10	Assembly, AGC/Cycle Detector	021569-4-1
A11	Assembly, Preset/Error Bypass	05153802
A12	Assembly, Reader Logic	021588-4-3
A13	Assembly, FWD/REV Control	021625-4-1
A15	Assembly, TOD Accumulator	021543-4-3
A16	Assembly, Buffer	021535-4-3
A17	Assembly, Code Generator	021554-4-1
A29	Assembly, Extender	021507-4-1
C1	Capacitor, 100 pF	100173
CR8,10,12	Diode, 6700	006700
R8	Resistor, 470 K 1/4W 5%	101630
R11	Resistor, 2.7 K 1/4W 5%	101599
R16	Resistor, 1.2 K 1/4W 5%	101581
R17	Resistor, 1 K 1/4W 5%	101569
	Card Rack, Front	08115501
	Card Rack, Rear	08115502
	Gusset, Left	041809-1-1
	Gusset, Right	041809-1-2
	Card Guide	021340-1-2

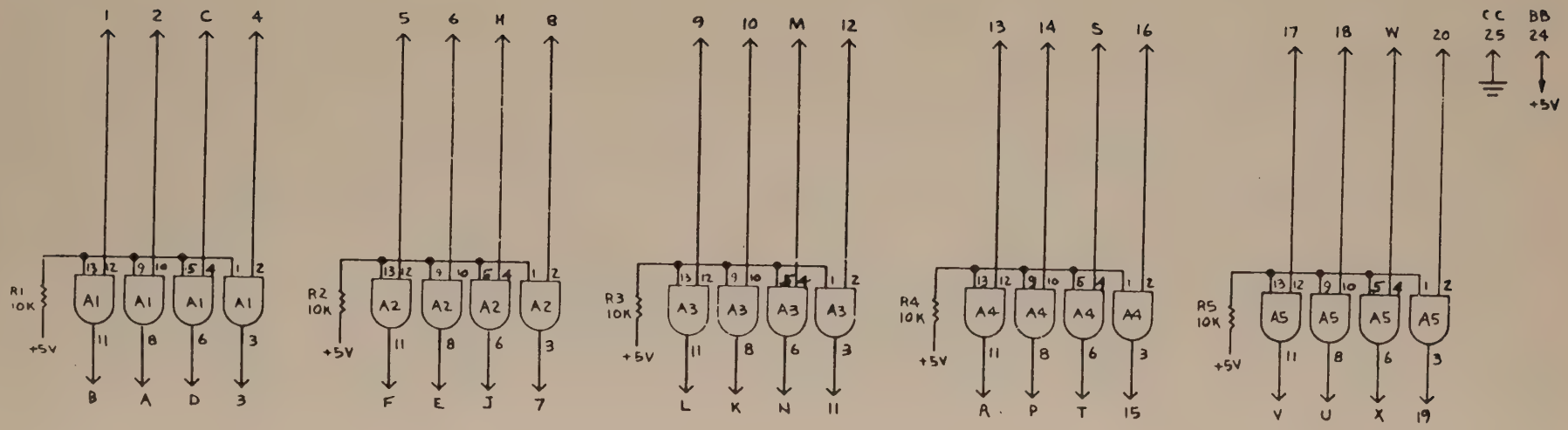
PARTS LIST
FINAL ASSEMBLY #06103402 (CON'T)

REFERENCE	DESCRIPTION	SD PART NO.
	TEST ASSEMBLY (CON'T)	#06115502
XA9-13,15-17,39	Connector, P.C. Edge	101204
XA101	Connector, Modification	051066-4-1
	Key	102653
P102	Shell	101263
	Standoff	100494
	Terminal, Male	10282202
	Spacer, Power Supply	051121-1-1
	FRONT PANEL ASSEMBLY REV C_1	#06115301
	Assembly, Display	041945-4-2
	Panel, Sub-Front	061171
	Panel, Nomenclature	061150
	Trim Strip	041773-1-1
DS1	Lamp, LED	100456
	Dress Nut	100893
S30	Switch, Rotary	06134401
S35	Switch, Toggle SPDT	102310
	Knob	102954
	REAR PANEL ASSEMBLY REV D	#06115401
	Rear Panel	041815-1-2
	Cover Plate, Oscillator	051913
B1	Fan	570899-0011
	Fan Screen	100886
	Cover Plate, 14 Pin	021398-1-1
	Cover Plate, 36 Pin	031124-1-1
	Cover Plate, 50 Pin	031394-1-1
	Hole Plug, BNC	100952
J3	Connector, 50 Pin	101136
J4	Connector, 14 Pin	101180
J8	Connector, BNC	101155
	Insulator, BNC	100823
	Washer, Fiber	101074
S1,15	Switch, Cover Plate	05120801
S16	Switch, Cover Plate	05120802
	#6 Flat Washer	100704

CIRCUIT DESCRIPTION
BUFFER ASSEMBLY
SCHEMATIC #021535-7-3 REV A_1

1) GENERAL

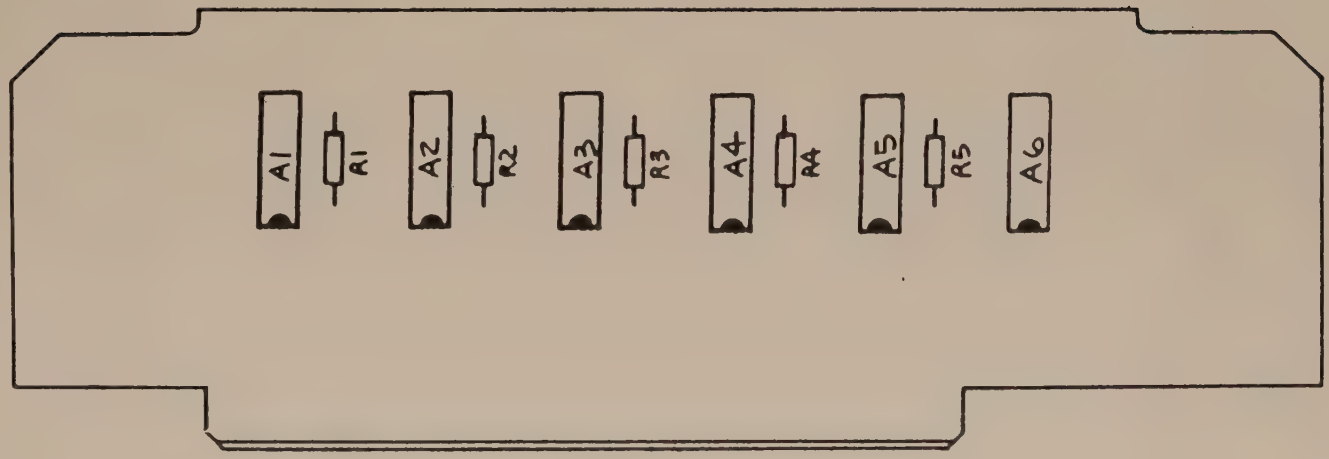
This card contains 20 integrated-circuit gates, connected as non-inverting buffers. It is used to buffer the seconds through hours outputs of the Time-of-Day Accumulators A binary "1" output is 5 V (±0.5V) 6 K source. A binary "0" outputs is 0 V (±0.5V) 12 mA sink.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, 1/4W, 5%.
2. PIN 14 OF ALL I.C.'S IS CONNECTED TO +5V & PIN 7 " " " " " " GRD.
3. A1 THRU A5 ARE MC1806P

BUFFER SCHEMATIC #021535-7-3 REV A_1



BUFFER ASSEMBLY #021535-4-3

PARTS LIST

BUFFER #021535-7-3 REV A_2

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly Schematic	021535-4-3 021535-7-3
A1-5	Integrated Ckt, MC1806P	025733
R1-5	Resistor, 10K ¼w 5%	101570
	Extractor	100865
	Roll Pin	100752

CIRCUIT DESCRIPTION

TIME-OF-DAY ACCUMULATOR

SCHEMATIC #021543-7-3

1) GENERAL

This card successively divides the 1 pps signal to provide outputs which represent seconds through hours. All outputs are buffered, an input inhibit circuit is provided, and the dividers are recycled to zero one second after reaching 23:59:59.

2) DIVIDERS

Dividers U1, U4, U7 and U8 are divide-by-10 circuits. Dividers U3 and U5 are divide-by-8 circuits. Recycle circuits formed from gates on U13 and U17 convert U1, U3 to a scale of 60, U7, U8 to a scale of 60 and U7, U8 to a scale of 24. Each divider has its data inputs, connected to a preset time source. Grounding the appropriate preset line will load the preset time into divider. Grounding pin 23 resets the Accumulator through gates on U9, U13 and U17.

3) RECYCLE CIRCUITS

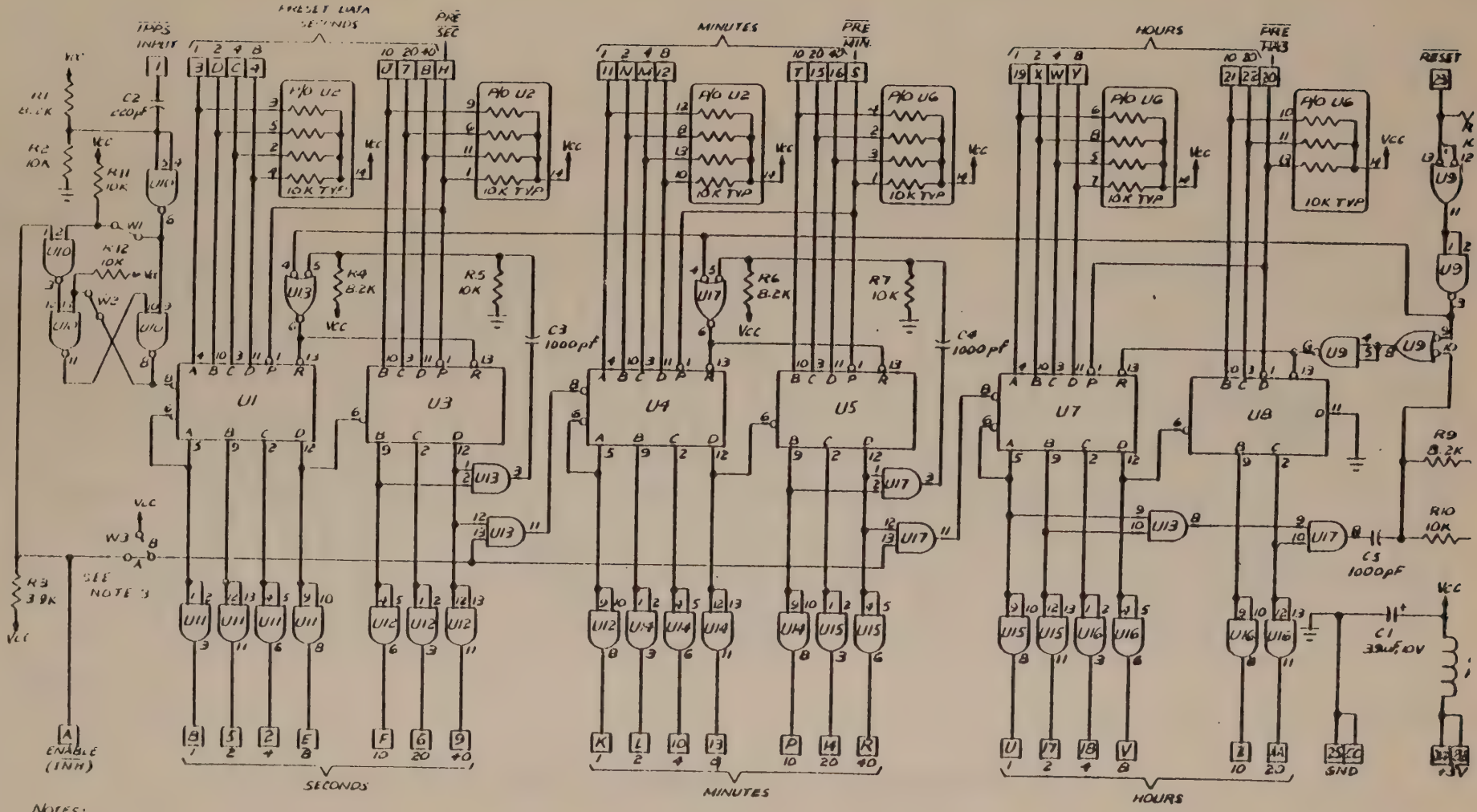
The scale of 60 recycle circuits for seconds and minutes are identical. The seconds circuit consists of AND gate U13-9 and a differentiating circuit formed from C3, R4 and R5. Gate U13-9 output goes high when U3 reaches a count of 5. It resets U1 and U3 through C3 and U13-6 when it returns low at the next count.

The scale of 24 recycle circuit for hours consists of AND gates U13-8, U17-8 and a differentiating circuit formed from C5, R9 and R10. The output from U17-8 goes high when U7 and U8 reach a count of 23. It resets U7 and U8 through C5 and U9-8,6 in tandem when it returns low at the next count.

4) INHIBIT CIRCUIT

The inhibit circuit is used to stop updating of the accumulator when the unit is in HOLD. Gate U10-6 inverts the 1pps input. Gates U10-8,11 form an RS flip-flop. Gate U10-3 inverts the $\overline{\text{INHIBIT}}$/ENABLE line, pin A. When this line is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$/ENABLE input.

Programming jumper W3 is installed in the "A" position in Readers and Reader/Generators to prevent update of minutes and hours in reverse read operation. It is installed in the "B" position in Clocks and Generators where the ENABLE input to Pin A is used for $\overline{\text{HOLD}}$.



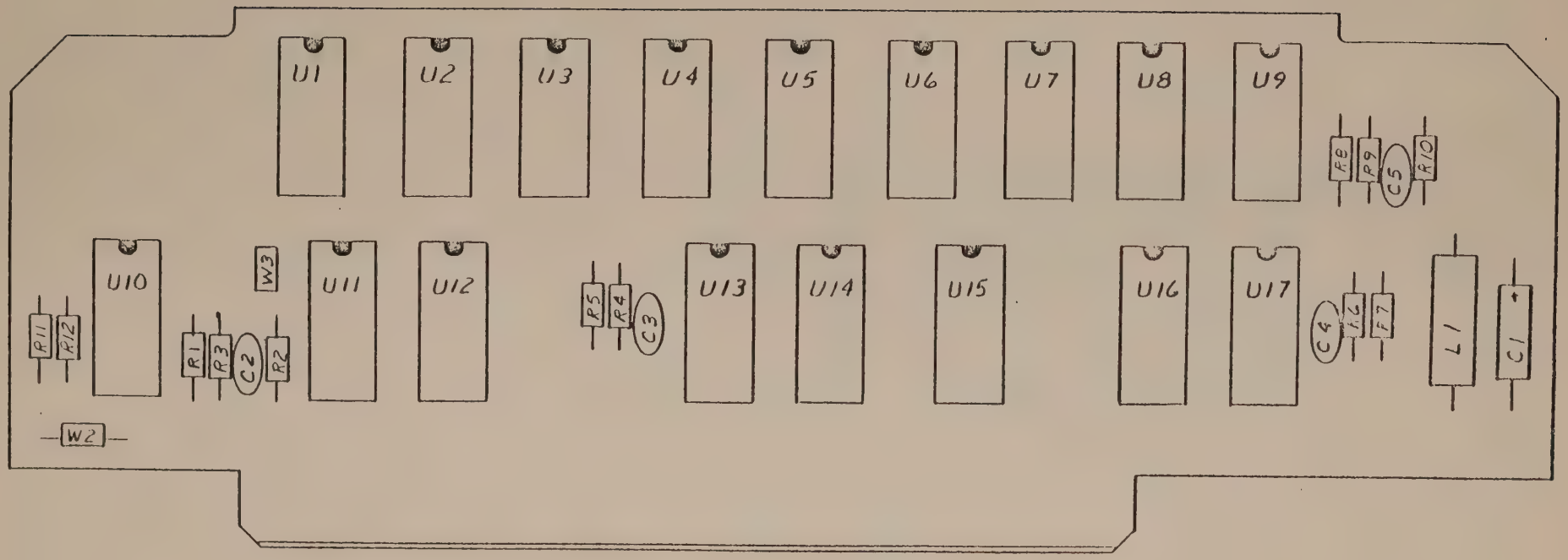
NOTES:

1. RESISTORS ARE ¼W, 5%, CARB. COMP.
2. I.C.'S

		VCC	GND
U1, U4, U7, U8	74LS196	14	7
U2, U6	RES PACK (10K)	14	–
U3, U5	74LS197	14	7
U9	74LS132	14	7
U10	806	14	7
U11, U12, U13, U14, U15, U16, U17	7408	14	7

3 PROGRAMMING JUMPER W3 IS INSTALLED IN THE "A" POSITION IN READER & READER/ GENERATORS TO PREVENT UPDATE OF HOURS & MINUTES IN REVERSE READ. IT IS INSTALLED IN THE "B" POSITION IN CLOCKS & GENERATORS WHERE THE ENABLE INPUT TO PIN A IS USED FOR HOLD

TOD ACCUMULATOR SCHEMATIC #021543-7-3 REV F



TOD ACCUMULATOR ASSEMBLY #021543-4-3 REV E

PARTS LIST
TIME-OF-DAY ACCUMULATOR #021543-7-3 REV F

REF.	DESCRIPTION	SD PART NO.
	Assembly	021543-4-3
	Schematic	021543-7-3
C1	Capacitor, 39 µF	100183
C2	Capacitor, 220 pF	117633
C3,4,5	Capacitor, 1000 pf	117639
R1,4,6,9	Resistor, 8.2K ¼w 5%	10159501
R2,5,7,8,10,11,12	Resistor, 10K ¼w 5%	10157001
R3	Resistor, 3.9K ¼w 5%	10160101
U1,4,7,8	Integrated Ckt, 74LS196	103164
U2,6	10K Resistor Pack	117241
U3,5	Integrated Ckt, 74LS197	103165
U9	Integrated Ckt, 74LS132	116946
U10	Integrated Ckt, 846	019716
U11 - U17	Integrated Ckt, 7408	103093
L1	Inductor, R45-4	101313
W2	Molded Jumper	102879
W3	Shorting Jack Mod.	08126101
	Shorting Jack	116979
	Pin, Swage	116978
	Extractor	100865

CIRCUIT DESCRIPTION
CODE GENERATOR
SCHEMATIC #021554-7-1

1) GENERAL

The IRIG DC Code Generator card can be used to generate the IRIG A, B, C, E, or H codes. Code selection may be remotely controlled or fixed by the particular card configuration. Days information may be optionally included and provision is made for the insertion of control function bits and/or straight binary seconds from a source external to the card. The following description is intended to apply in general to all configurations of the card. The specific assembly used is identified by the attached assembly, schematic and parts list.

2) DIVIDER CIRCUITS

Refer to the timing diagrams and the schematic for this and subsequent sections. Divider A8 is a divide-by-two, then-by-five counter which divides down the "Z" RATE" and provides decoded outputs for the code generating gates. Divider A15 is a divide-by-five, then-by-two counter which takes the output of A8, divides it down and supplies decoded outputs for the scan gates and the code generating gates. Divider A17 is a divide-by-two, then-by-six counter. Its principle function is to control the secondary scan gate A4. The divide-by-twelve is used only for IRIG C, the divider being reset at the count of ten or by the sync input for the other codes. This early reset is shown on the timing diagram as A18-8. The reset pulse is quite short and therefore has been widened for clarity. The area between the dotted lines on Sheet two is simply eliminated when the divider resets at ten. Reset at ten is established by gate A18-8. A one-shot (A18-12,6) performs code frame reset. The external reset signal (pin Z) may be used for code frame reset when W1 is installed, or the card can supply a reset pulse to synchronize the associated accumulator when W2 is installed.

Divider A7 (if present) is a divide-by-five counter provided for external use. It is synchronized with the other divider chips.

3) SCAN GATES

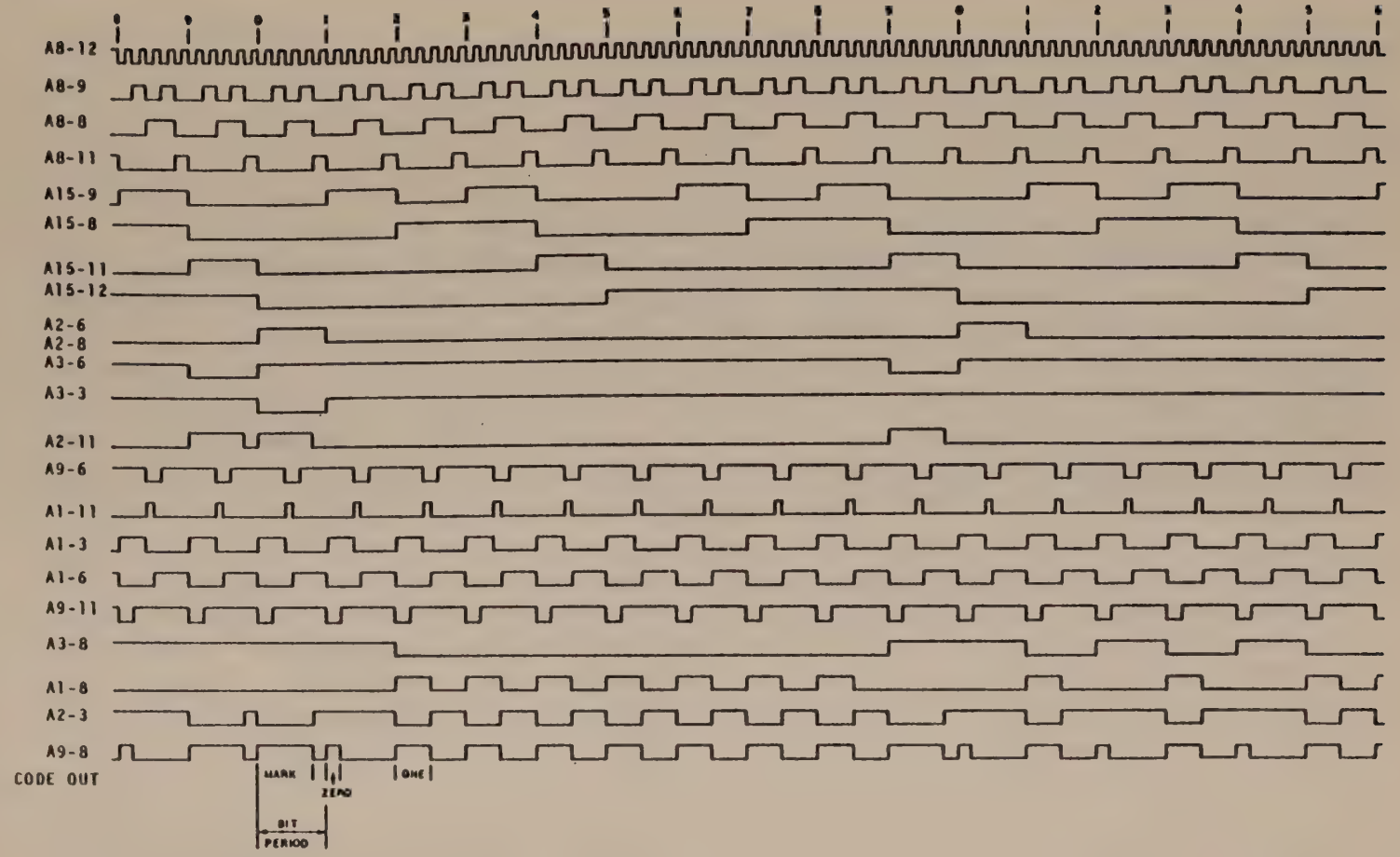
Creation of serial ONES is accomplished by a two-stage switching network and a series of gates. Chips A10-A14 are basically single pole (pin 8 is the output), 8-position switches. The inputs to these switches are the time data from the system accumulator. (One or more of these chips may be deleted on a particular card configuration.) The switching is controlled by BCD information on pins 1, 2 and 13. Since the above switches have the BCD inputs in parallel, all the time decades will provide outputs simultaneously; thus, the need for

switch A4. This switch, controlled from the BCD outputs of divider A17, selects the proper time interval for serializing each switch output. (The series of gates associated with A14 and A13, if present, further control these switches which may have outputs that should not be present in certain codes.) For example, tenths-of-seconds are added only in IRIG A, units-of-seconds are deleted in IRIG E, and all seconds information is deleted in IRIG C. Gates A5-8, A5-11 and A3-8 are used to inhibit the presence of serials ONES at certain times when no serial ONES should be present. This prevents the spurious ONES (coming from the switches) from appearing in the output code.

4) CODE GENERATING GATES

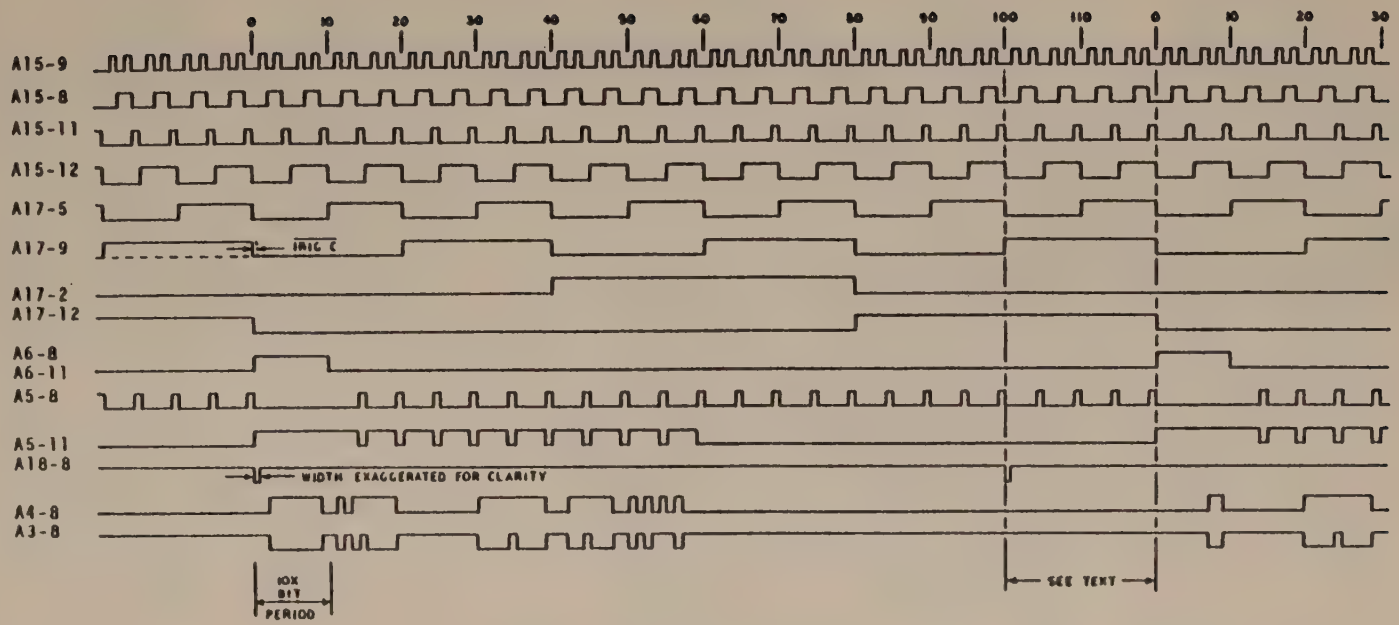
These gates must generate three time intervals in a 2:5:8 ratio. The time for the intervals is dependent on the bit period and is determined by the "Z RATE" on pin 2. A "2" length is a ZERO, a "5" is a ONE, and an "8" is an INDEX MARKER.

The INDEX MARKERS are generated by gating the output of divider A15. Gate A1-3 adds information from the output of divider A11 to create the "8" width. Gates A6-8 and A6-11 allow an extra pulse from gates A2-6 and A2-8 to give the "double mark" at the start of the frame. Gate A3-6 provides the marker at each tenth frame interval. Gate A9-11 supplies a pulse of "2" width at the start of each bit interval. If a MARKER or a ONE is not present, then the output code will be high for only the "2" width. Gate A1-6 supplies the "5" width pulse. This is AND-gated with the $\overline{\text{SERIAL ONES}}$ from A3-8 by gate A1-8. (External bits may be inserted on this same line through pin 22.) The presence of a ONE will cause the "5" width to appear in the output code, masking the "2" width which is always present. Gates A2-3 and A9-8 are used to combine the various widths to produce the output code at pin B.



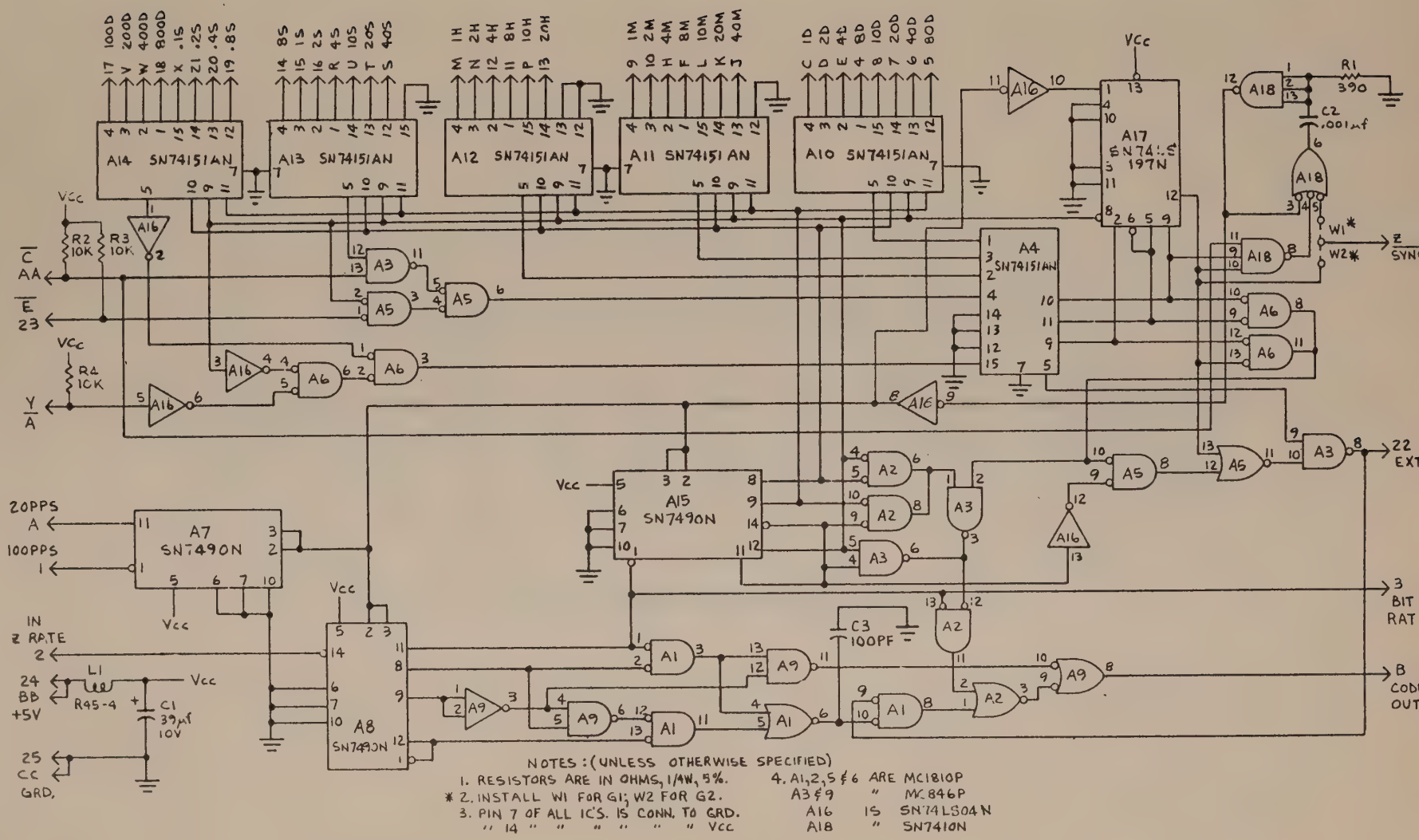
NOTE
CODE SHOWN IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 1 of 2)

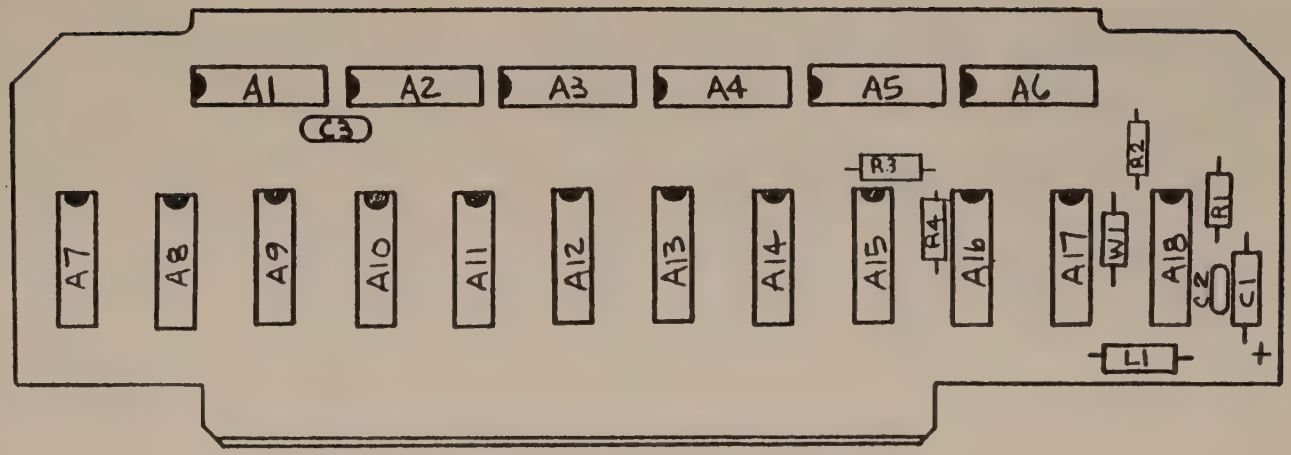


NOTE:
CODE SHOWN (SERIAL ONES & A18-8) IS ARBITRARY AND NOT NECESSARILY REALIZABLE.

IRIG DC CODE GENERATOR - TIMING DIAGRAM - (Sheet 2 of 2)



CODE GENERATOR SCHEMATIC #021554-7-1 REV F



CODE GENERATOR ASSEMBLY #021554-4-1 REV E

PARTS LIST
CODE GENERATOR #021554-7-1 REV E

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021554-4-1
	Schematic	021554-7-1
A1,2,5,6	Integrated Ckt, MC1810P	025735
A3,9	Integrated Ckt, MC846P	019716
A4,10-14	Integrated Ckt, 74151	02577101
A7,8,15	Integrated Ckt, 7490	025732
A16	Integrated Ckt, 74LS04	103749
A17	Integrated Ckt, 74LS197	103165
A18	Integrated Ckt, 7410	019706
C1	Capacitor, 39 µF, 10V	100183
C2	Capacitor, .001 µF	100076
C3	Capacitor, 100 pF, DM15	100173
L1	Inductor, R45-4	101313
R1	Resistor, 390Ω ¼w 5%	101592
R2-4	Resistor, 10K ¼w 5%	101570
W1	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
AGC/CYCLE DETECTOR
SCHEMATIC #021569-7-1

1) GENERAL

The AGC/Cycle Detector card contains two separate and independent circuits. The first circuit (AGC) provides automatic gain control for the incoming signal. The second circuit (Cycle Detector) generates three control signals: Upper Large Cycle, Lower Large Cycle, and Each Cycle.

2) AGC

Serial time-code input (from the tape unit, or other source), pin 19, is applied to a voltage divider network which consists of R12 and FET Q1. The bias on the gate of Q1 determines the ratio of the divider network and therefore the signal level at the gate of Q2. Q2 is a source follower providing high input impedance (so as not to load the divider network) and low impedance to drive differential amplifier A5. The input to A5 is applied to the "+" input (pin 3) via C10 for noninverting operation, as applicable to the particular circuit configuration).

A5 is provided with negative feedback through R20 for a maximum gain of about 40dB, and two "roll-off" networks C13-R22, and C12 to ensure stability. Pins T, Y, and A are normally connected by an external jumper. When optional filter networks are used, they are connected between pins T and Y.

The amplified signal is applied to the base of Q4 which controls the emitter voltage of Q3. Q4 and Q3 form a signal peak-detection circuit which provides the AGC control voltage to the gate of Q1. The output on pin T is set from 2 to 2.5 V p-p through the AGC potentiometer R4.

3) CYCLE DETECTOR

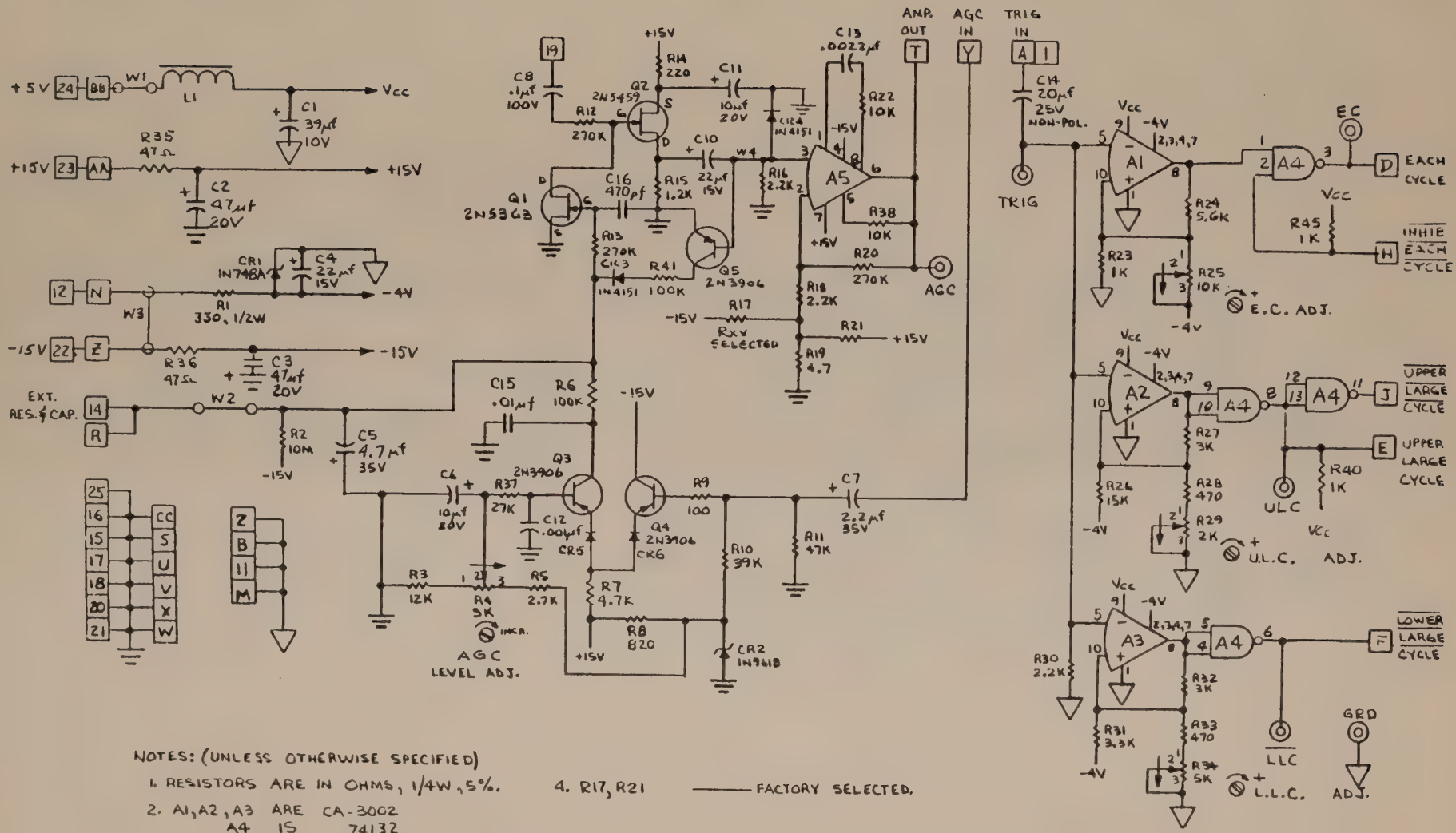
The output of amplifier A5 is also applied to three cycle-detector circuits, A1, A2 and A3.

A1 triggers at the zero-axis crossing and will generate a square wave at the input carrier frequency. The hysteresis of this trigger circuit is adjustable by means of the EC ADJ. potentiometer, R25.

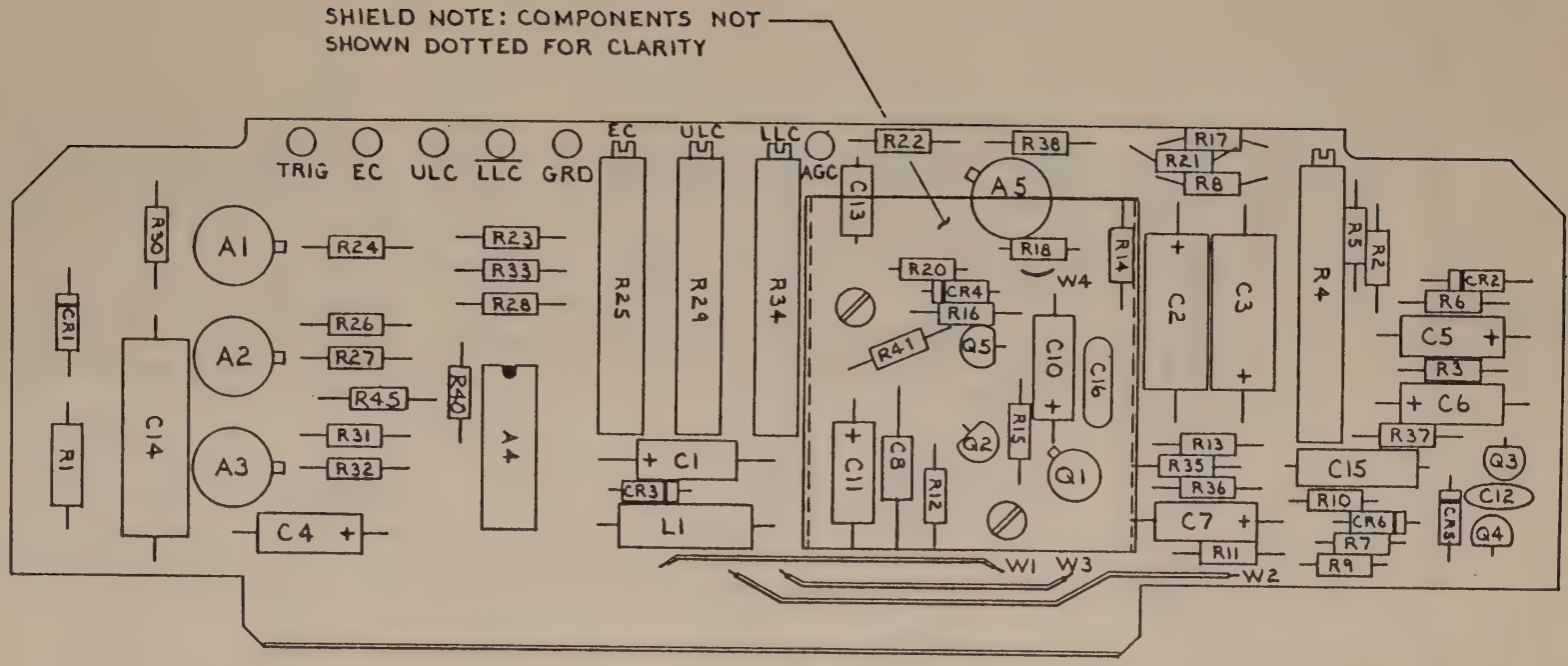
A2 and A3 generate output pulses only upon receipt of a Large Half Cycle; A2, the Upper Large Cycle and A3 the Lower Large Cycle.

These two amplifiers will initiate their signals when the input signal reaches about 75% of the Large Half Cycle amplitude and will terminate them when the input signal reaches zero. The trigger points are adjustable by means of the ULC ADJ. and LLC ADJ. potentiometers, R29 and R34.

Saturating logic amplifiers, A4-2, A4-4, and A4-6, serve to amplify, invert the signals, and to provide isolation. A4-8 and A4-12 are used to inhibit the EC output when the $\overline{\text{INH EC}}$ (pin H) is grounded.



AGC & CYCLE DETECTOR SCHEMATIC #021569-7-1 REV V



AGC & CYCLE DETECTOR ASSEMBLY #021569-4-1 REV Y

PARTS LIST

AGC & CYCLE DETECTOR #021569-7-1 REV Y

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021569-4-1
	Schematic	021569-7-1
A1-3	Integrated Circuit, CA3002	025701
A4	Integrated Circuit, SN74132N	045270
A5	Integrated Circuit, MC1439G	025729
C1	Capacitor, 39 µF, 10 V	100183
C2,3	Capacitor, 47 µF, 20 V	100186
C4,10	Capacitor, 22 µF, 15 V	100125
C5	Capacitor, 4.7 µF, 35 V	100071
C6,11	Capacitor, 10 µF, 20 V	100063
C7	Capacitor, 2.2 µF, 35 V	100100
C8	Capacitor, .1 µF, 100 V	100141
C12	Capacitor, .001 µF	100076
C13	Capacitor, .0022 µF	100185
C14	Capacitor, 20 µF, 25 V	100264
C15	Capacitor, .01 µF, 200 V	100168
C16	Capacitor, 470 pF, 100 V	117637
CR1	Diode, 1N749A	100419
CR2	Diode, 1N961B	100395
CR3-6	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
Q1	Transistor, 2N5363	101403
Q2	Transistor, 2N5459	101384
Q3-5	Transistor, 2N3906	101378
R1	Resistor, 330 Ω, 5%, 1/2 W	101474
R2	Resistor, 10 M, 5%, 1/4 W	101564
R3	Resistor, 12 k, 5%, 1/4 W	101565
R4,34	Potentiometer, 5 k, Beckman 78P, Var	101938
R5	Resistor, 2.7 k, 5%, 1/4 W	101599
R6,41	Resistor, 100 k, 5%, 1/4 W	101558
R7,32	Resistor, 4.7 k, 5%, 1/4 W	101598
R8	Resistor, 830 Ω, 5%, 1/4 W	101567
R9	Resistor, 100 Ω, 5%, 1/4 W	101609
R10	Resistor, 39 k, 5%, 1/4 W	101561
R11	Resistor, 47 k, 5%, 1/4 W	101574
R12,13,20	Resistor, 270 k, 5%, 1/4 W	101769
R14	Resistor, 220 Ω, 5%, 1/4 W	101566

PARTS LIST

AGC & CYCLE DETECTOR #021569-7-1 (Cont'd)

REFERENCE	DESCRIPTION	SD PART NO.
R15	Resistor, 1.2 k, 5%, 1/4 W	101581
R16,18,30	Resistor, 2.2 k, 5%, 1/4 W	101562
R19	Resistor, 4.7 Ω, 5%, 1/4 W	101796
R22,38	Resistor, 10 k, 5%, 1/4 W	101570
R23,40,45	Resistor, 1 k, 5%, 1/4 W	101569
R24	Resistor, 5.6 k, 5%, 1/4 W	101584
R25	Potentiometer, 10 k, Beckman 78P	101918
R26	Resistor, 15 k, 5%, 1/4 W	101552
R27	Resistor, 3 k, 5%, 1/4 W	101548
R28,33	Resistor, 470 Ω, 5%, 1/4 W	101625
R29	Potentiometer, 2 k, Beckman 78P	101876
R31	Resistor, 3.3 k, 5%, 1/4 W	101559
R35,36	Resistor, 47 Ω, 5%, 1/4 W	101560
R37	Resistor, 27 k, 5%, 1/4 W	101587
W1-4	Wire, #24 AWG Solid Bus	
	Shield, AGC	021421-1-1
	Spacer	100934
	Insulator	021427-1-1
	Extractor	100865

CIRCUIT DESCRIPTION
READER LOGIC
SCHEMATIC #21588-7-3

1) GENERAL

Signals, $\overline{\text{LLC}}$ and EC respectively, are connected to pins A and 1 of the Reader Logic Card. The Reader Logic circuit accepts the EC and $\overline{\text{LLC}}$ signals and detects the ONES, ZEROS, and MARKS in the code. These signals are used to shift the BCD time information of the input code into a shift register and then transfer it to the Time-of-Day Accumulator Card which drives the Display drivers and Code Generator.

2) FUNCTIONAL

The basic scheme is as follows:

When a MARK is detected, the nine-bit shift register (A14) and 1/2 (A13) is cleared and a ONE set in the first bit position. Also, the "Y" counter A10 is advanced one.

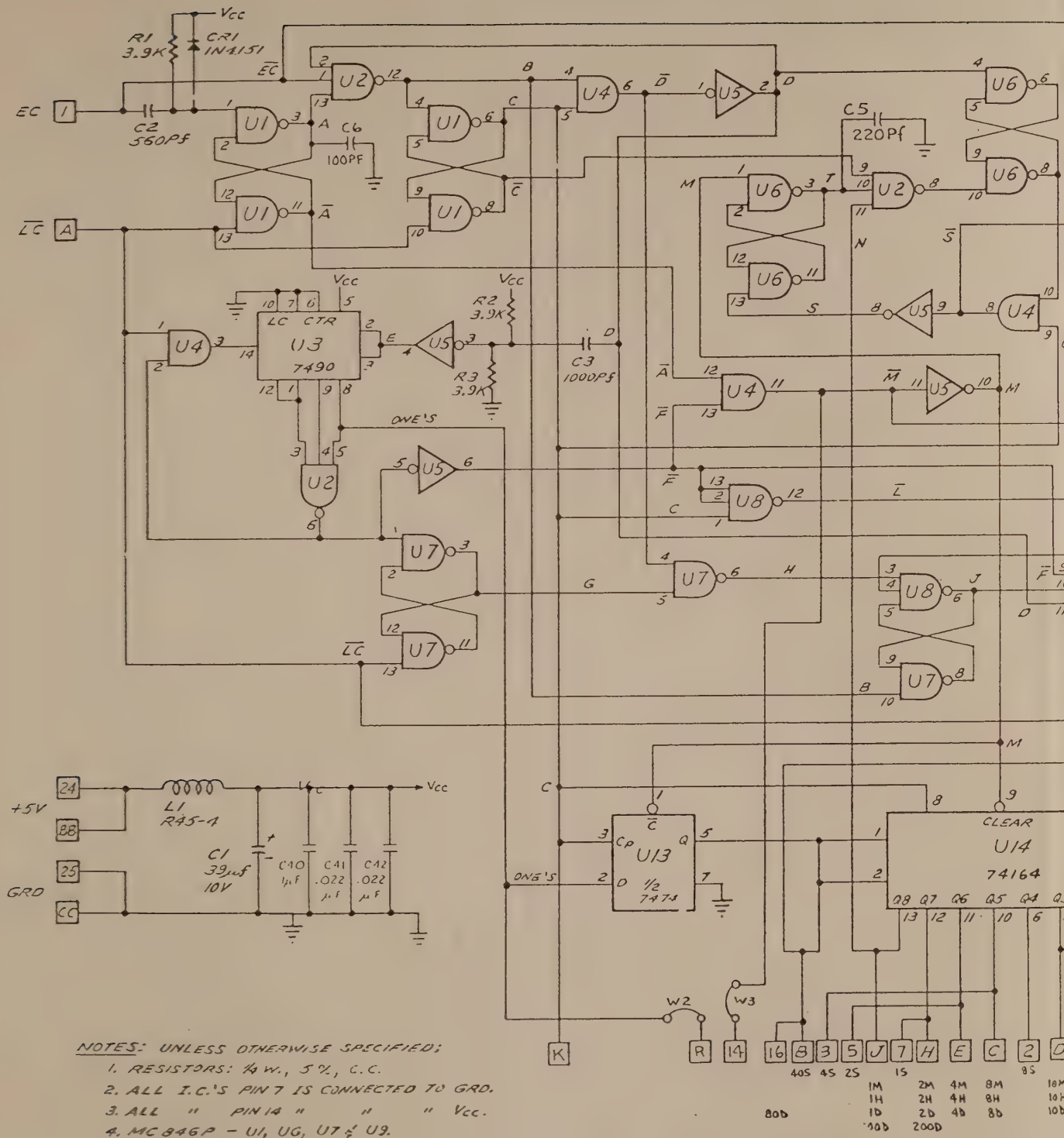
When the second MARK of the double MARK is detected, the sequence is changed so that the "Y" counter is set to ZERO if it was not already at ZERO. It is not advanced for this MARK. Nor is the shift register cleared. However, the ONE that was entered by the first MARK is shifted one position. The shift register is now advanced one position for each binary bit of the time frame. When the ONE that was entered by the first MARK reaches the ninth position, a circuit is set which permits the next shift signal to transfer the information from the register to the seconds section of the Time-of-Day Accumulator.

When the next MARK is detected, the register is cleared, a ONE entered and the "Y" counter advanced one. After nine bits are shifted into the register the information is transferred to the minutes section of the Accumulator. This cycle of operation is repeated a third time for hours information. If Days Option E20 is included, two additional cycles transfer this information to the Days Accumulator. The "Y" counter continues to count MARKS throughout the time frame.

When the first MARK of the next double MARK is detected, it steps the "Y" counter from 9 to zero advancing the Time-of-Day Accumulator one second. It is thus updated at the beginning of the frame and will contain the same information (assuming no errors) scanned in during the frame.

The readout does not change during scan-in since the Accumulator is already updated.

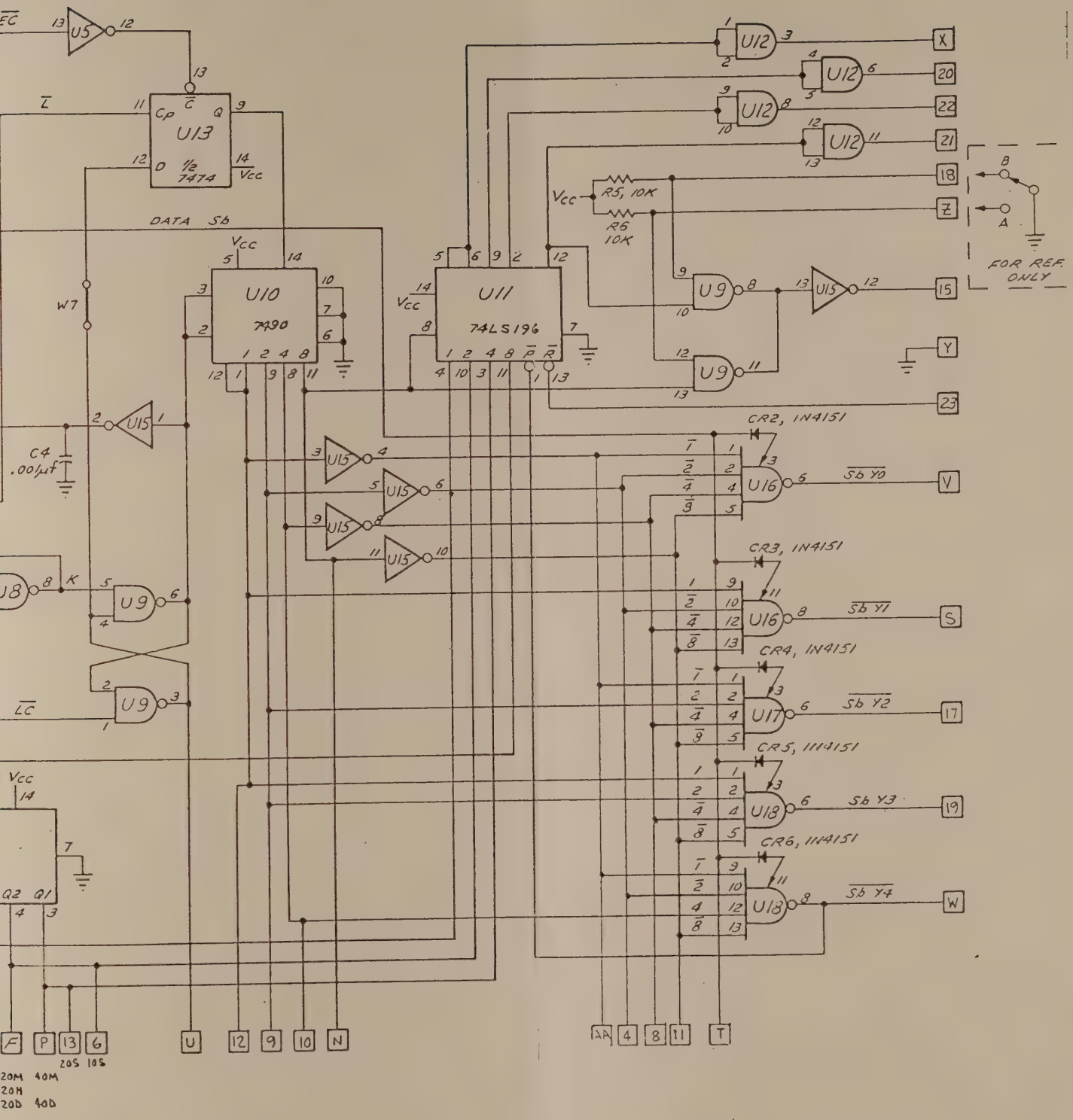
The serial level shift code at pin R is fed to the Error Bypass circuit where it is compared with the output from the Code Generator which represents, in serial form, the contents of the Time Accumulator.



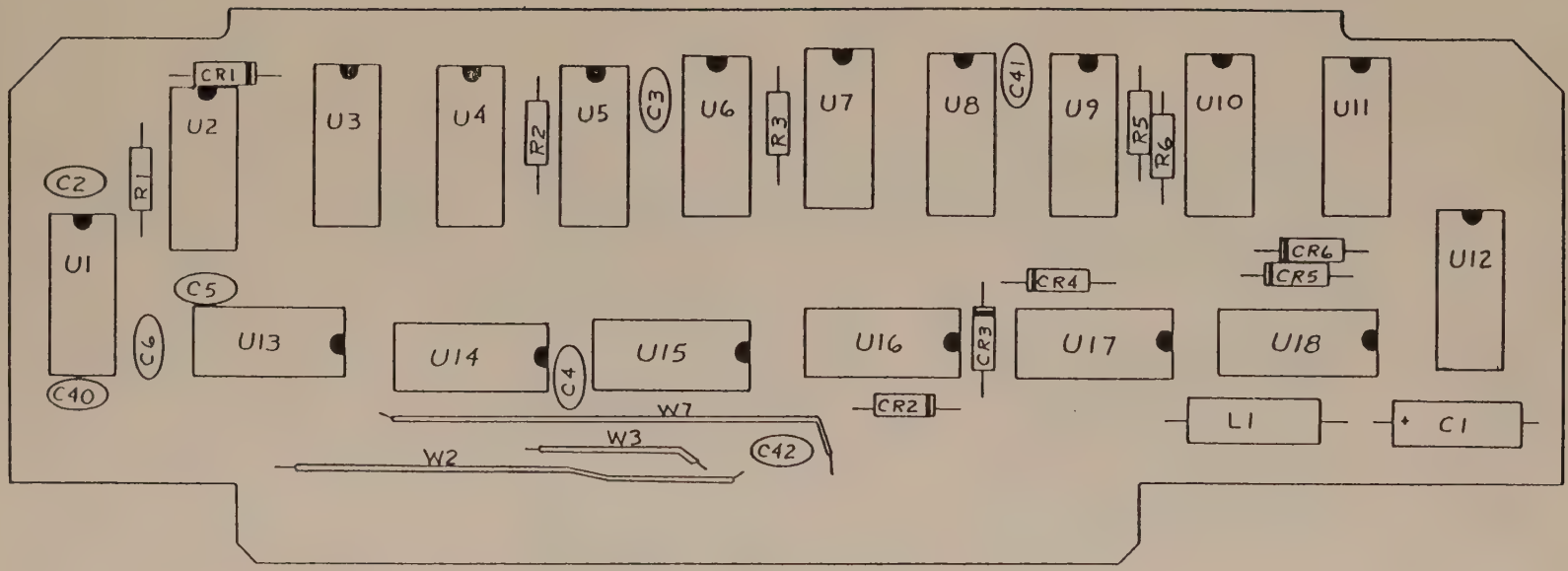
NOTES: UNLESS OTHERWISE SPECIFIED;

1. RESISTORS: ¼ W., 5%, C.C.
2. ALL I.C.'S PIN 7 IS CONNECTED TO GRD.
3. ALL " PIN 14 " " " Vcc.
4. MC 846P – U1, U6, U7 & U9.
   MC 862P – U3 & U8.
   MC 1806P – U4 & U12.
   MC 836P – U5 & U15.
   MC 830P – U16, U17 & U18.

READER LOGIC SCH



MATIC #021588-7-3 REV. F



READER LOGIC ASSEMBLY #021588-4-3 REV C

PARTS LIST

READER LOGIC #021588-7-3 REV D

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly, Reader Logic	021588-4-3
	Schematic, Reader Logic	021588-7-3
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 560 pF, Mica	100222
C3	Capacitor, .001 µF, DM15	100243
C4	Capacitor, .001 µF, Disc	100076
C5	Capacitor, 220 pF, DM15	100220
C6	Capacitor, 100 pF	100173
C40	Capacitor, 1.0 µF, 50 V	100176
C41,42	Capacitor, .022 µF, 25 V	106483
CR1-6	Diode, 1N4151	100385
L1	Inductor	101313
R1-3	Resistor, 3.9 k, 1/4 W, 5%, CC	10160102
R5,6	Resistor, 10 k, 1/4 W, 5%, CC	10157002
U1,6,7,9	Integrated Circuit, MC846P	019716
U2,8	Integrated Circuit, MC862P	019719
U3,10	Integrated Circuit, 7490	025732
U4,12	Integrated Circuit, MC1806P	025733
U5,15	Integrated Circuit, MC836P	025704
U11	Integrated Circuit, 74LS96	103164
U13	Integrated Circuit, 7474	025241
U14	Integrated Circuit, 74164	025751
U16,17,18	Integrated Circuit, MC830P	019712
W2,3,7	Wire, Insulated, 24GA	
	Extractor	100865

CIRCUIT DESCRIPTION
FWD/REV CONTROL
SCHEMATIC #021625-7-1

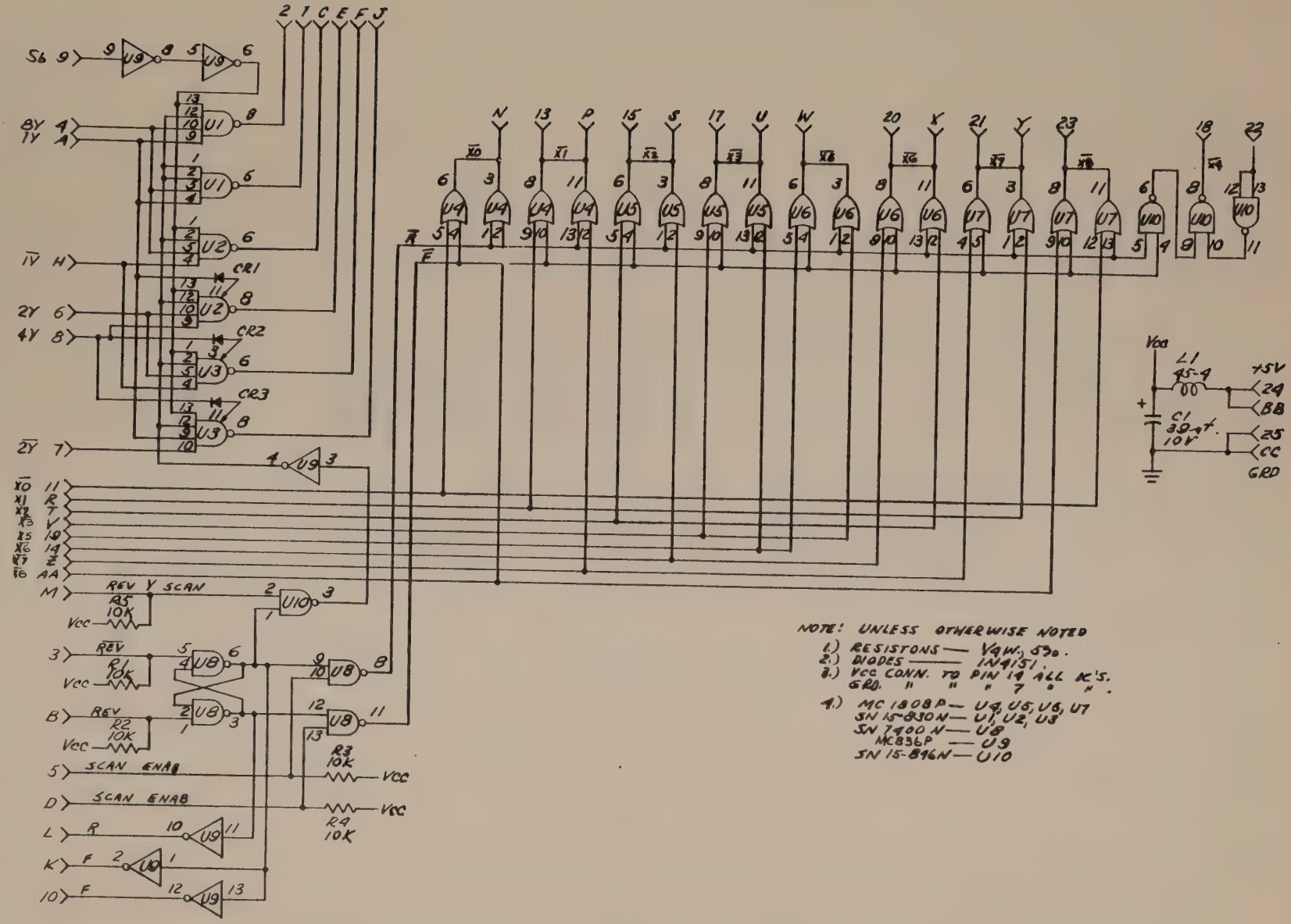
1) GENERAL

The FWD/REV Control Card, A13 contains gates which invert the order of the time data bits stripped from the input code when reading a reverse code. In addition, it provides buffered forward and reverse control signals and establishes the Y-Strobe signals needed to load data into the Time Accumulator when operating with a reverse code. This circuitry is active only when operating in one of the search modes. All circuits are disabled in the PRESET and GEN Modes.

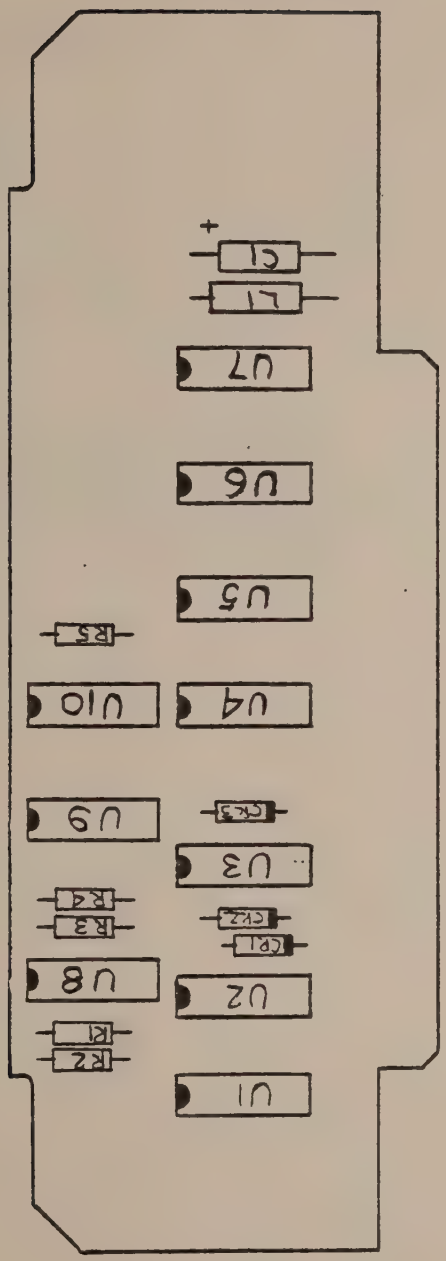
2) OPERATION

Referring to Schematic #021625-7-1, the FWD and REV signals from the Tape Search section are fed to pins 3 and B, respectively. When operating in reverse (tape transport moving in a reverse direction) the FWD (REV) signal is at ground, and the $\overline{\text{REV}}$ signal is positive. Flip-flop U8-6/3 is set. The positive output from U8-6 is fed to 4 circuits: 1) through U10-3 and U9-4, opening Y Strobe Scan gates U1,U2 and U3; 2) through U8-8, opening gates U4-3, U4-11, U5-3, U5-11, U6-3, U6-11, U7-3 and U7-11 to negative time data signals $\overline{\text{X0}}$ through $\overline{\text{X8}}$; 3) through U9-2 to the Error Bypass circuit, disabling forward Y Scan; and 4) through U9-12, clamping the Z-Rate signal at ground, thus blocking update of the TOD Accumulator (A15) and inhibiting operation of the Code Generator A17) and Modulator (A8) circuits. The Y Strobe Scan gates load the rearranged data bits into the TOD Accumulator (A15) as each frame is stripped from the input code.

When forward operation is established, flip-flop U8-6/3 is reset. The Y Strobe Scan gates are disabled (all outputs driven positive), gates U4-6, U4-8, U5-6, U5-8, U6-6, U6-8, U7-6 and U7-8 are open (time data restored to normal order); U9-12 and U9-2 outputs are up, restoring normal operation of the TOD Accumulator, Code Generator, Modulator and Error Bypass circuitry.



FWD/REV CONTROL SCHEMATIC #C21625-7-1A



FWD/REV CONTROL ASSEMBLY #A21625-4-1A

PARTS LIST

RWD/REV CONTROL #021625-7-1 REV A_1

REF.	DESCRIPTION	SD PART NO.
	Assembly	021625-4-1
	Schematic	021625-7-1
C1	Capacitor, 39 µF, 10 V	100183
CR1-3	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1-5	Resistor, 10 k 5%, 1/4 W	101570
U1-3	Integrated Circuit, SN15830N	019712
U4-7	Integrated Circuit, MC1808P	025734
U8	Integrated Circuit, SN7400N	019705
U9	Integrated Circuit, MC836P	025704
U10	Integrated Circuit, SN15846N	019716
	Extractor	100865

CIRCUIT DESCRIPTION
MINOR COUNTER
SCHEMATIC #21632-7-2

1) GENERAL

The Minor Counter card can provide up to three serial decades with common reset, parallel preset and two sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. Provision is included for three output pulse rates with 10% duty cycle which may be supplied in place of the days recycle circuit.

2) DECADE DIVIDERS

The up to three decade dividers are connected in tandum. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. Jumpers W1 and W2 permit the data strobe associated with the center decade (A4) to be wired in common with the data strobe input to the first decade (A1) or the third (A6). The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through two sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. One of the two sets (A10,A13 and A15) can be gated by inputs through pin L,K and J, respectively. These gate lines are buffered by inverters on A11.

4) INPUT INHIBIT CIRCUIT

This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flip.

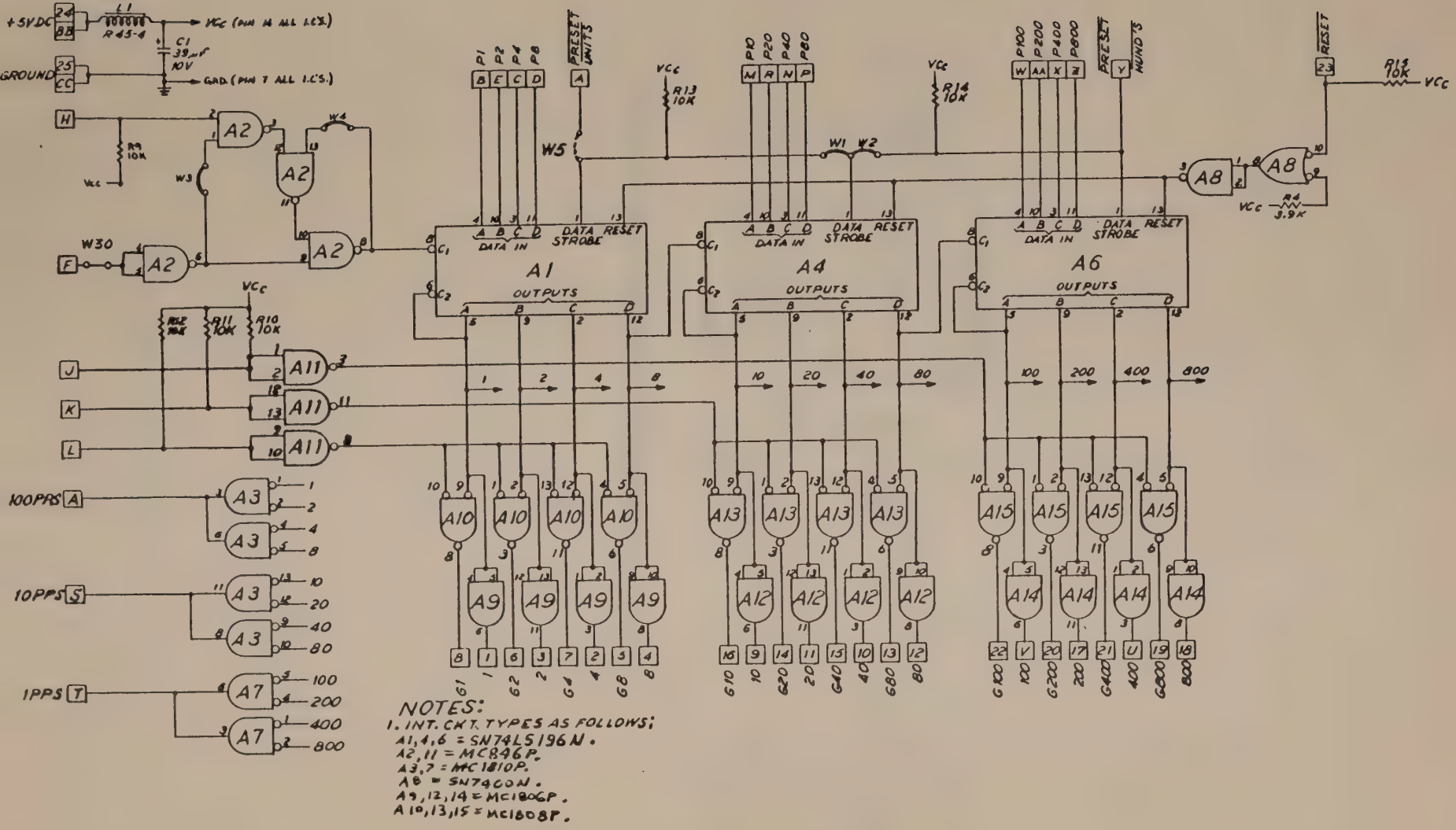
A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8,11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

5) OUTPUT PULSE RATES

Three sets of gates are used to produce three 10% duty cycle pulse rates. Each pulse goes high when the four outputs from the corres-

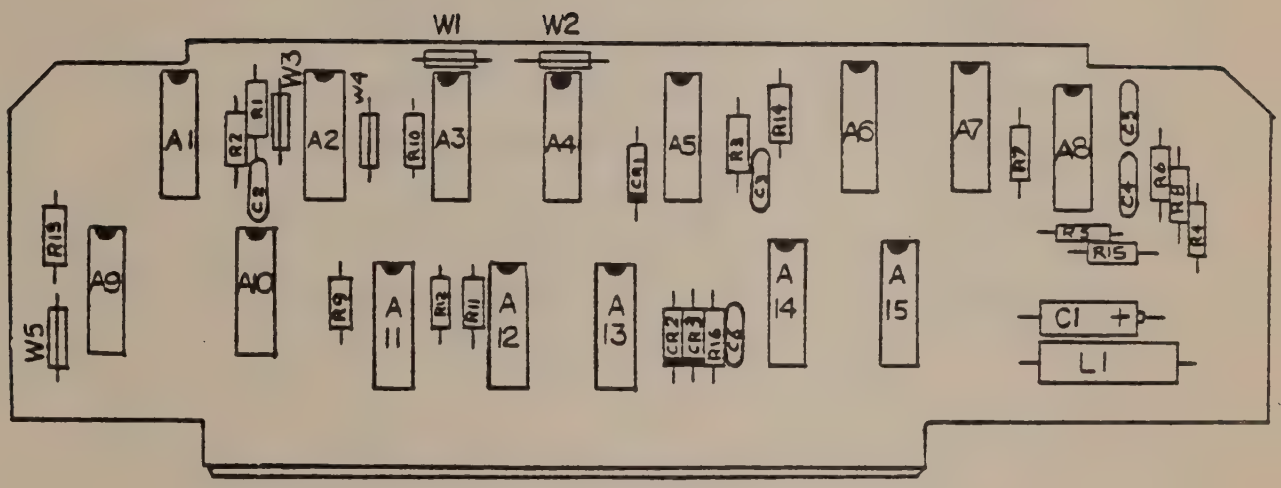
ponding decades are low (leading edge on time). The pulse remains up until the output of the decade in 001. Thus, the pulse is high 10% of the time. The output is a 5 V logic level behind 6 kΩ.

The pulse rate outputs are fed to pins A, S and T which are used for units preset and days recycle inputs on other configurations of the card. Chip A5 is removed when the rate outputs are supplied.



NOTES:
1. INT. CKT. TYPES AS FOLLOWS;
A1,4,6 = SN74LS196N.
A2,11 = MC846P.
A3,7 = MC1810P.
A8 = SN7400N.
A9,12,14 = MC1806P.
A10,13,15 = MC1808P.

3 DIGIT ACCUMULATOR BUFFER SCHEMATIC #021632-7-2 REV D



DAYS ACCUMULATOR ASSEMBLY #021632-4-1 REV C

PARTS LIST

MINOR COUNTER #021632-7-2 REV F

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	021632-4-1
	Schematic	021632-7-2
A1,4,6	Integrated Ckt, 74LS196	103164
A2,11	Integrated Ckt, MC846P	019716
A3,7	Integrated Ckt, MC1810P	025735
A8	Integrated Ckt, 7400	019705
A9,12,14	Integrated Ckt, MC1806P	025733
A10,13,15	Integrated Ckt, MC1808P	025734
C1	Capacitor, 39 µF, 10 V	100183
L1	Inductor, R45-4	101313
R9,10-15	Resistor, 10 K 1/4 W 5%	10157002
R4	Resistor, 3.9 K 1/4W 5%	10160102
W1-W4	Jumper, Molded	102879

CIRCUIT DESCRIPTION

PRESET AND ERROR BYPASS
SCHEMATIC #7-051538

1. GENERAL

This card contains Preset Control, Error Bypass, Pulse Rate, Z-Rate, FWD/REV, and Reset circuits. It is used in the Model 8132 Reader, the Model 8134 Reader/Search Unit, the Model 8152 Generator/Reader and the Model 8154 Generator/Reader/Search Unit.

2. OPERATION

PRESET CONTROL: Referring to the lower right corner of the schematic, Preset Logic is provided for detecting TOD and Days Coincidence in the Model 8154 Time Code Generator/Reader/Search Unit. When armed in the PRESET Mode, these circuits combined with the comparator, detect coincidence between the time entered on the front panel PRESET/START TIME thumbwheel switches and the contents of the accumulator. The coincidence signals are sent to preset control circuits on Time Base and Control Card A27. When Days/ID Option E13 is included, these circuits separate the Days and TOD sections of the comparator providing separate Days and TOD Coincidence outputs to Card A27.

ERROR BYPASS: The Error Bypass circuit is shown at the top of the schematic. It is enabled in the READ Forward Mode of Operation only and includes provision for selecting 0,3,5,7 or 9 frames of Error Bypass. This means that data stripped from the input code will not be loaded into the Accumulator until after the selected number of consecutive error frames has been counted. (READ Reverse is equivalent to "0" error bypass in which all data are loaded into the Accumulator irrespective of errors.)

The Error Bypass circuit accepts the serial level shift output from the Reader Logic Card and compares it with the serial level shift output from the Code Generator Card in exclusive OR gate U13-11. The output from this gate is fed to gate U7-6 along with blanking and sampling signals which differ as a function of the code being read and the options present in the Reader.

The sampling signal from U14-2 is developed in Counter/Decoder U1/U2 from the Z-Rate input and selected by U3.

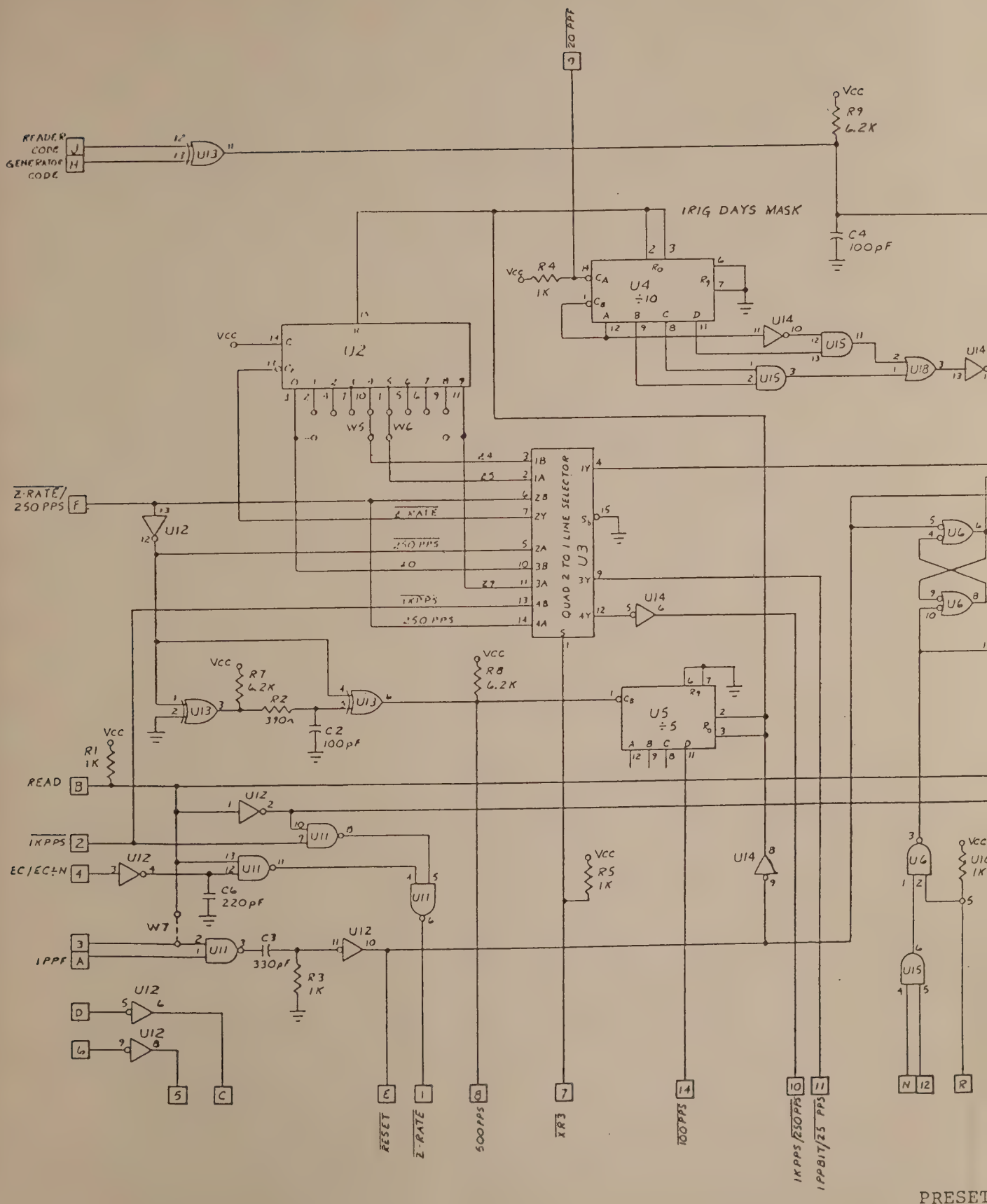
The IRIG Days Mask from U14-12 is developed by Counter U4 and associated decoding gates from the 20 ppF input to pin 9. It inhibits comparison of days bits so that readers without the Days Option can read IRIG Codes containing days.

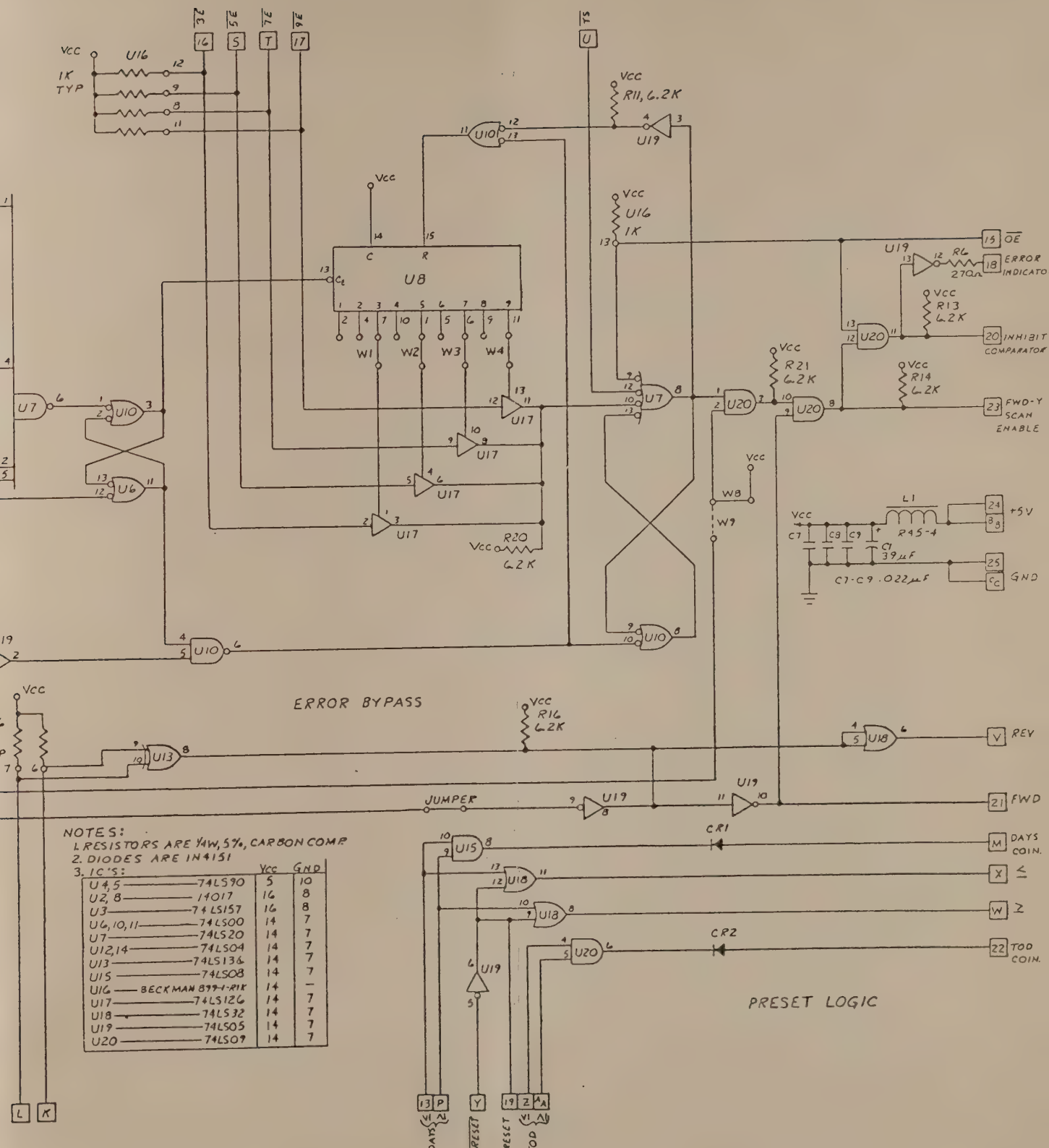
The blanking signal from flip-flop U6-6, 8 restricts comparison to that portion of the code containing time information. It is set by the differentiated leading edge of the 1 ppF input through U11-3, C3, U12-10 ($\overline{\text{RESET}}$), and cleared by the output from the 3 input NAND gate formed from U15-6 and U6-3. The $\overline{\text{RESET}}$ signal clears flip-flop U10-3/U6-11, provided it was set by the detection of at least one error (U7-6 output going low) during the previous frame. Assuming that no error has occurred, this flip-flop will not be set and output U6-11 will be high opening gate U10-6. When the clear signal from U6-3 occurs during the current frames, it is inverted by U19-2 and fed through U10-6 resetting counter U9 and flip-flop U7-8/U10-8. The low output from U7-8 is fed through U20-3 and U20-8 to pin 23 and the Reader Logic Card, inhibiting forward Y-Scan. (Gates U20-3, 8 are open in READ Forward only.) This same signal is fed through U20-11 to pin 20. The resulting output is used to enable the comparators in tape search units. Now, if an error occurs during the next frame, flip-flop U10-3/U6-11 will be set (with U10-3 high and U6-11 low) and, when U6-3 output goes low during the frame, U10-6 will be closed and counter U9 will not be reset.

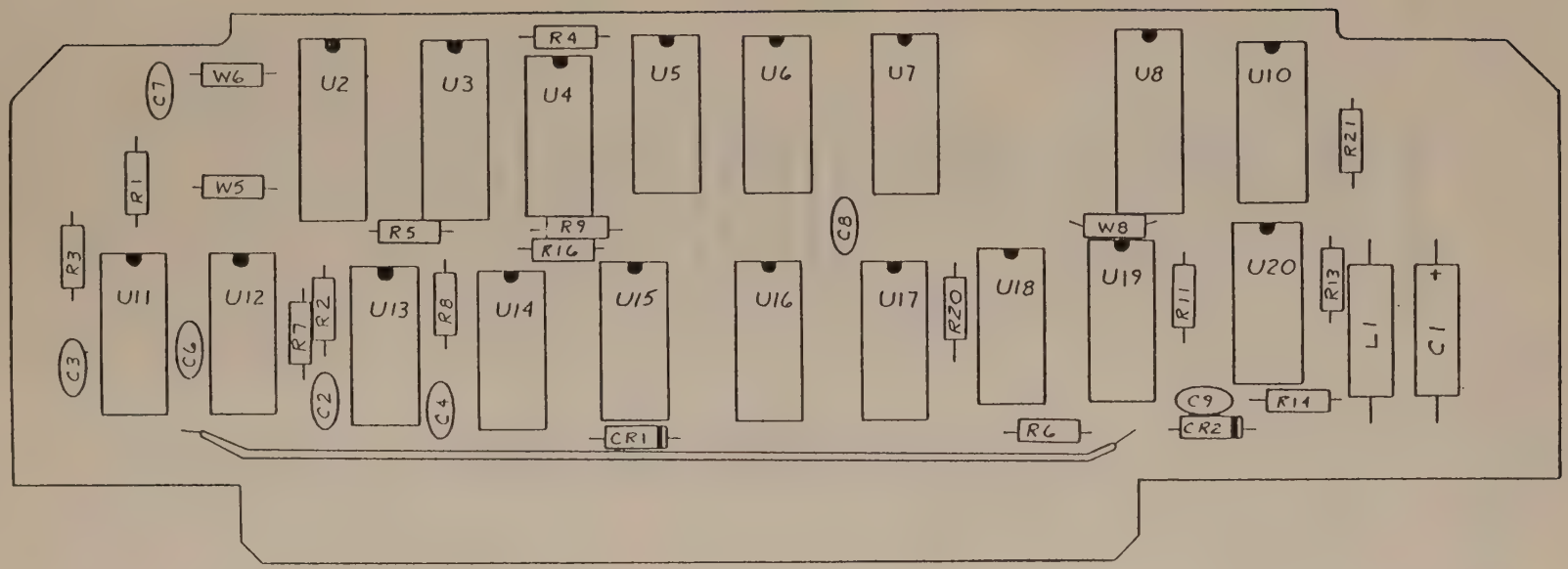
The $\overline{\text{RESET}}$ signal at the start of the next frame clears flip-flop U10-3/U6-11 and counter U9 accumulates one count. If the next frame is good, U9 is reset and the count starts over. If the next frame is bad, however, U9 accumulates a second count. The BCD outputs from counter U9 are decoded by U8 and fed to a set input to flip-flop U7-8/U10-8 through gates on U17 which are used to select the desired number of error bypass frames. When counter U9 reaches this number, flip-flop U7-8/U10-8 is set enabling forward scan of the time data (stripped from the input code by the Reader Logic during the next frame) into the Accumulator. The tape search comparators, when present, are inhibited by the output from U20-11 during this one frame. Counter U9 is reset through U19-4 and U10-11 and the sequence starts again. The selected number of consecutive error frames must occur before the input time data is permitted to be loaded into the Accumulator.

PULSE RATES: Selected pulse rates from U3 through U14-4 and U14-6 and from edge detectors U13-3,6 and counter U5 are provided as outputs when XR3 Time Codes are being read.

Z-RATE and RESET: These circuits, shown at the lower left on the schematic, select Z-Rate output from GENERATE and READ and develop a $\overline{\text{RESET}}$ pulse from the leading edge of the 1 ppF input.


READER CODE GENERATOR CODE
J
H
U13
20 PPF
Vcc
R9
6.2K
IRIG DAYS MASK
C4
100pF
R4
1K
U4
÷10
U14
U15
U18
U2
W5
W6
U3
QUAD 2 TO 1 LINE SELECTOR
Z-RATE/
250 PPS
F
U12
Z-RATE
250 PPS
10
IKPPS
250 PPS
R7
6.2K
R2
390Ω
C2
100pF
R8
6.2K
U5
÷5
R1
1K
READ
B
IKPPS
Z
EC/EC±N
4
C6
220pF
W7
1PPF
A
C3
330pF
R3
1K
U11
R5
1K
D
G
5
C
E
RESET
1
Z-RATE
8
500PPS
7
XR3
14
100PPS
10
1K PPS/250PPS
11
1PPBIT/25 PPS
U6
U16
N
12
R
PRESET


ERROR BYPASS
PRESET LOGIC
JUMPER
NOTES:
1. RESISTORS ARE ¼W, 5%, CARBON COMP
2. DIODES ARE IN4151
3. IC'S:
U4,5 — 74LS90 — Vcc 5 — GND 10
U2,8 — 14017 — 16 — 8
U3 — 74LS157 — 16 — 8
U6,10,11 — 74LS00 — 14 — 7
U7 — 74LS20 — 14 — 7
U12,14 — 74LS04 — 14 — 7
U13 — 74LS136 — 14 — 7
U15 — 74LS08 — 14 — 7
U16 — BECKMAN 899-1-R1K — 14 — —
U17 — 74LS126 — 14 — 7
U18 — 74LS32 — 14 — 7
U19 — 74LS05 — 14 — 7
U20 — 74LS09 — 14 — 7
U8
W1
W2
W3
W4
R11, 6.2K
R20 6.2K
R21 6.2K
R14 6.2K
R13 6.2K
R16 6.2K
R6 270Ω
R45-4
C1 39μF
C7-C9 .022μF
ERROR INDICATO
INHIBIT COMPARATOR
FWD-Y SCAN ENABLE
+5V
GND
REV
FWD
DAYS COIN.
TOD COIN.
CR1
CR2
DAYS PRESET
PRESET
PRESET
TOD PRESET



PRESET/ERROR BYPASS ASSEMBLY #05153802 REV C

PARTS LIST

PRESET AND ERROR BYPASS #051538

REFERENCE	DESCRIPTION	PART NO.
	Assembly	051538XX
	Schematic	7-051538XX
C1	Capacitor, 39 µF, 10 V	608114-0396
C2,3	Capacitor, 100 pF	601110-0101
C4	Capacitor, 330 pF	601110-0331
C6	Capacitor, 220 pF	601110-0221
C7-9	Capacitor, .022 µF	601005-0223
CR1,2	Diode, 1N4151	7011N4151
L1	Inductor, R45-4	570080-0003
R1,3,4,5	Resistor, 1 K, 1/4 W, 5%	651102-0102
R2	Resistor, 390 Ω 1/4 W, 5%	651102-0391
R6	Resistor, 270 Ω 1/4 W, 5%	651102-0271
R7-16	Resistor, 6.2 K, 1/4 W, 5%	651102-0622
R40	Resistor, 6.2 K, 1/8 W	651111-0622
U4,5	Integrated Ckt, 74LS90	703SN74LS90N
U2,8	Integrated Ckt, 14017	703MC14017BP
U3	Integrated Ckt, 74LS157	703SN74LS157N
U6,10,11	Integrated Ckt, 74LS00	703SN74LS00N
U7	Integrated Ckt, 74LS20	703SN74LS20N
U12,14	Integrated Ckt, 74LS04	703SN74LS04N
U13	Integrated Ckt, 74LS136	703SN74LS136N
U15	Integrated Ckt, 74LS08	703SN74LS08N
U16	1 K Resistor Pack	654013-0102
U17	Integrated Ckt, 74LS125	703SN74LS125N
U18	Integrated Ckt, 74LS32	703SN74LS32N
U19	Integrated Ckt, 74LS05	703SN74LS05N
U20	Integrated Ckt, 74LS09	703SN74LS09N
	Extractor	506020-2030

CIRCUIT DESCRIPTION
POWER SUPPLY
SCHEMATIC #041810-7-9

1) GENERAL

The power supply provides four regulated dc voltages (±5 V and ±15 V), five unregulated dc voltages (±9 V, ±21 V and +210 V), and an 18 V rms time base output at the line frequency. The regulated output voltage levels are adjustable. These outputs are current limited and are short-circuit-proof to ground. (Note: Overheating may result if a short is maintained over an extended period of time.) Both voltage-sense and sense-return lines are provided for the regulated outputs. These lines are wired to provide regulation at the load. Fuses are provided for the unregulated +21 V and +210 V on the power supply assembly.

Input power is 115/230 V, 48 to 440 Hz at less than 100 W with nominal line and all outputs fully loaded. (Note: The line frequency may be limited, 48 to 62 Hz unless Option L12 is utilized, by the fan characteristics if a fan is included in the unit.) Input power is fed to transformer T1 through line filter Z1, fuse F1, a front panel power switch and 115/230 select switch, S101. The third wire is grounded to the chassis.

The transformer is constructed with split-primary windings which are connected in parallel for 115 V operation and in series for 230 V operation. Selection is made by 115/230 switch, S101. (Note: Units are normally shipped in the 115 V configuration with a 2A Slo-Blo fuse, F1. If the unit is converted to 230 V operation, F1 should be changed to 1A Slo-Blo.) Three secondary windings (two with center taps) are provided, one for ±9 V, one for ±21 V and 18 V rms, and the third for +210 V.

2) NONREGULATED SUPPLIES

The +210 V nonregulated supply is developed by the bridge rectifier formed from diodes CR5 through CR8, plus the filter circuit formed from R1, R2 and C5. The resulting output is fed through F2 (0.125A) to P103, pins 18 and V. It is used to drive front panel numerical indicating tubes and is rated at 100 mA.

The ±21 V nonregulated supplies are developed by bridge rectifier CR1 through CR4 and filtered by C1, C2, C8 and C11. The +21 V output is used internally as the source for the +15 V regulator. It is fed through F3 (1A) to P103, pins 15 and S, where it is available for use as a relay supply. The -21 V output is used internally as the source for the -15 V regulator, and to power both the -15 V and -5 V regulator amplifiers. It is also available at P103, pin 4, for external use. Each of the ±21 V supplies is rated at 0.5A.

The 18 V rms is derived from the secondary winding which provides the ac voltage to develop the ±21 V. This rms voltage is fed through R15 to P103 pins 22 and Z.

The +9 V nonregulated supply is developed by full-wave rectifier CR11, CR12 and filtered by C3, C4 and C10. It is used internally as the source for the +5 V regulator, and to power both the -15 V and -5 V regulator amplifiers. It is available at P103, pins 21 and Y, for external use as a lamp supply. It is rated at 4A.

Tge -9 V nonregulated supply from full-wave rectifier CR9, CR10 and filter C6 is used internally as the source for the -5 V regulator. It is available at P103, pin 2, for external use. It is rated 0.5A.

3) REGULATED SUPPLIES

The regulated +15 V, 0.5A output at P103, pin N, is established through pass transistor Q1 under the control of regulator U1 and the divider network (R4, R5, R6) between the +15 V SENSE line (P103, pin 12) and ground. The voltage on the arm of 15 V ADJ potentiometer (R5) is fed to U1 where it is compared with the internal reference, referred to the 15 V sense-return line (P103, pin 8). The current limit is imposed by sensing the drop across R9 and the circuit is stabilized by network R32, C7.

The regulated -15 V, 0.5A output at P103, pin 5, is established through Q2 and Q3 under the control of regulator amplifier U3-12. It uses the +15 V SENSE line as the reference, comparing it with the output through R10, R11 and the -15 V supply.1 Potentiometer R5 serves as the adjustment for both outputs. Current is limited by cutting the base drive to Q2 when the drop across R14 approaches one diode drop.

The regulated +5 V, 4A output at P103, pins P and R, is established through Q4 and Q5 under the control of regulator U2 and a divider network (R18, R19). The +5 V SENSE line at P103, pins 13 and 14, is compared with the fraction of the U2 internal reference voltage appearing on the arm of 5 V ADJ potentiometer (R19). The current limit is imposed by sensing the drop across R24 through divider R22, R23. The circuit is stabilized by network R33, C12. The regulated -5 V, 0.5A output at P103, pin C, is established through Q6 and Q7 under the control of regulator amplifier U3-10. It uses the +5 V SENSE line as reference, comparing it with the output through R26, R27 and the -5 V SENSE line at P103, pin 3. The -5 V output tracks the +5 V supply and potentiometer R19 adjusts both. Output current is limited by cutting the base drive to Q6 when the drop across R30 approaches one diode drop.

4) CALIBRATION PROCEDURE

Test Equipment: see Chapter 4.

Check that fuse F1 is the proper size for the input voltage selected:

2 A, 115 V

1 A, 230 V

With an input of 115 V ac (230 V is so equipped) ±5%, 50/60 Hz.

Check the following at the Power Supply P.C. Board edge connector:

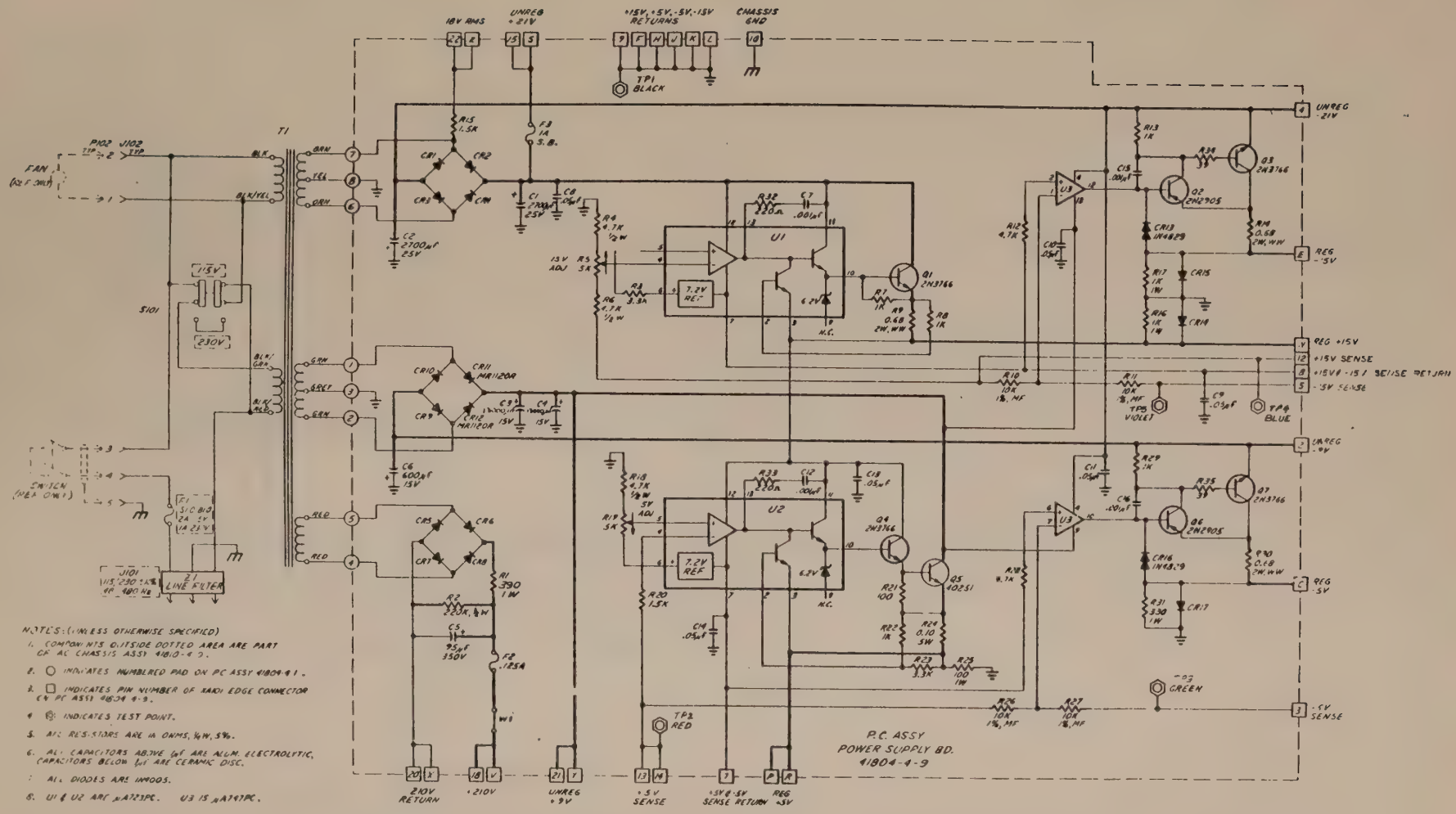
1) +210 V ±25% at pins V, 18 (GND 20, X)
2) +21 V ±20% at pins S, 15 (GND BLACK TEST POINT)
3) +9 V ±20% at pins Y, 21 (GND BLACK TEST POINT)
4) -9 V ±20% at pin 2 (GND BLACK TEST POINT)
5) -21 V ±20% at pin 4 (GND BLACK TEST POINT)

Measure the +15 V supply on the BLUE (GND BLACK) Test Point and adjust R5 (15 V ADJ) for +15 V ±0.3 V.

Measure the -15 V supply on the VIOLET Test Point and verify that it is within ±0.3 V of -15 V. Readjust R5 if necessary so that both +15 and -15 V supplies are within ±0.3 V.

Measure the +5 V supply on the RED Test Point and adjust R19 (5 V ADJ) for 5 V ±0.1 V.

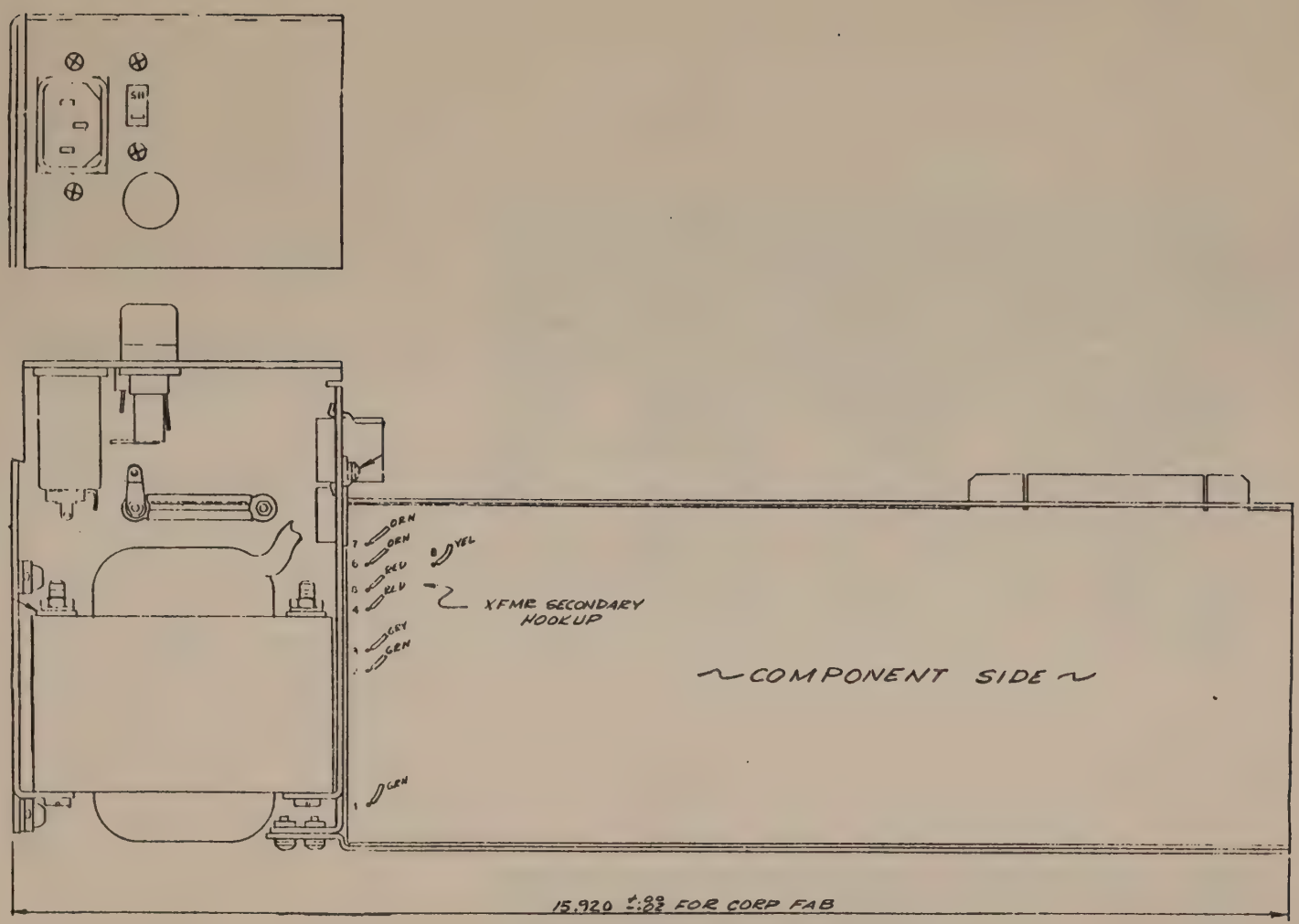
Measure the -5 V supply on the GREEN Test Point and verify that it is within ±0.1 V of -5 V. Readjust R19 if necessary so that both +5 and -5 V supplies are within ±0.1 V.



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENTS OUTSIDE DOTTED AREA ARE PART OF AC CHASSIS ASSY 41810-4-2.
2. ○ INDICATES NUMBERED PAD ON PC ASSY 41804-4-1.
3. □ INDICATES PIN NUMBER OF CARD EDGE CONNECTOR ON PC ASSY 41804-4-3.
4. ⊗ INDICATES TEST POINT.
5. ALL RESISTORS ARE IN OHMS, ¼W, 5%.
6. ALL CAPACITORS ABOVE 1μF ARE ALUM. ELECTROLYTIC. CAPACITORS BELOW 1μF ARE CERAMIC DISC.
7. ALL DIODES ARE IN4005.
8. U1 & U2 ARE μA723PC. U3 IS μA747PC.

POWER SUPPLY
SCHEMATIC #041810-7-9 REV C1

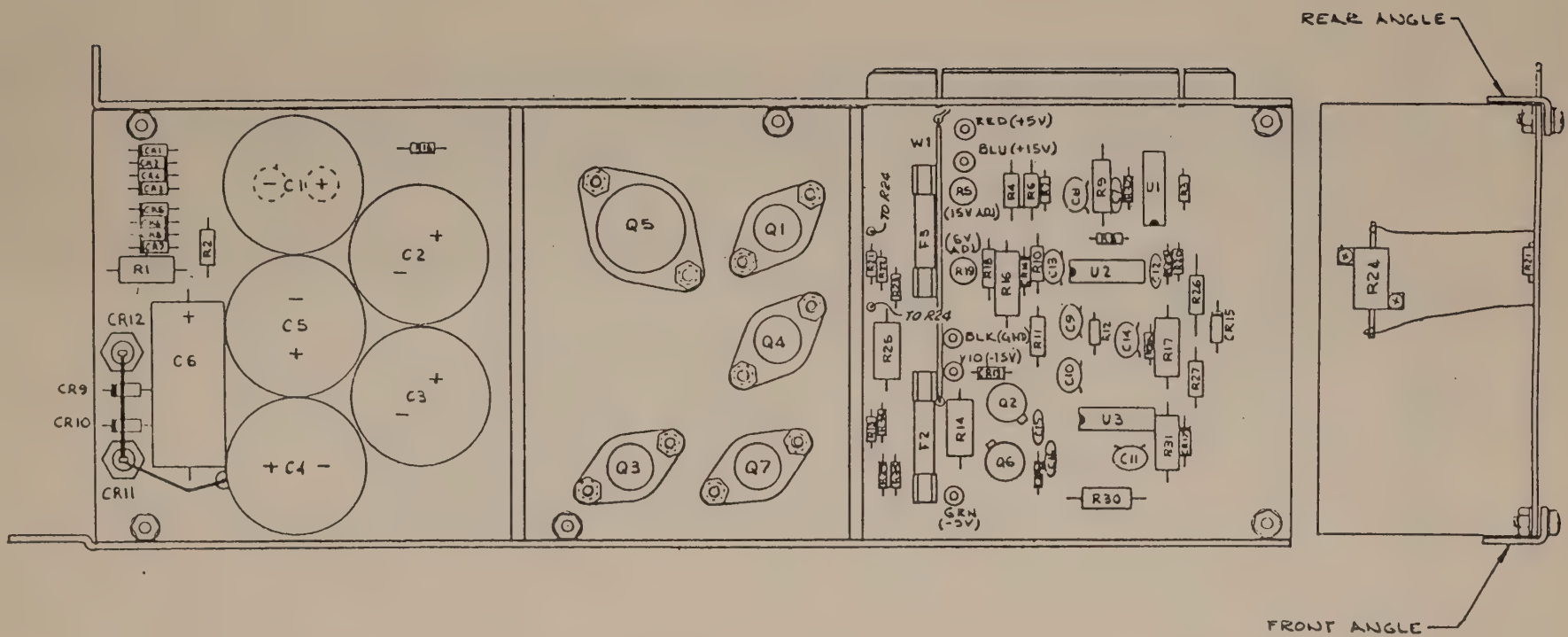


POWER SUPPLY ASSEMBLY #041810-4-9 REV A

PARTS LIST

POWER SUPPLY ASSEMBLY #041810-4-9 REV A_1

REF.	DESCRIPTION	SD PART NO.
	Assembly	041810-4-9
	Schematic	041810-7-9
	Assembly, Power Supply Board	041804-4-9
J101/Z1	Line Filter/Power Input	102461
J102	Connector Shell, 5 contacts	101264
F1	Fuse, 2A Slow-Blow, 115 V	100585
S101	Switch, Slide	102331
T1	Transformer	021408-6-1
XF1	Fuse, Post	102409
	Contact, Female (J102)	10282201
	4-40 x 7/16 PHMS	10062607
	4-40 x 1/4 PHMS	10062604
	#4 Flat Washer	100703
	#4 Kep Nut	100941
	Ground Lug	100486
	#10-32 x 2.75 PHMS	10064444
	#10 Fiber Washer	100684
	Grommet	100885
	4-point Terminal Strip	100084
	6-32 x 5/16 FHMS	10073105
	#6 Kep Nut	100862
	6-32 x ¼ PHMS	10063204
	#6 Split Lock Washer	100712
	Power Supply Cable	041810-3-6



POWER SUPPLY REGULATOR ASSEMBLY #041804-4-9 REV C,

PARTS LIST

POWER SUPPLY BOARD #041804-4-9 REV H

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	041804-4-9
	Schematic	041810-7-9
C1,2	Capacitor, 2700 µF, 25 V	100232
C3,4	Capacitor, 13,000 µF, 15 V	116074
C5	Capacitor, 95 µF, 350 V	100259
C6	Capacitor, 600 µF, 15 V	100258
C7,12,15,16	Capacitor, .001 µF, 1 kV, Disc	100076
C8-11,13,14	Capacitor, .05 µF, 50 V, Disc	100134
CR1-10,14,15,17	Diode, 1N4005	100413
CR11,12	Diode, MR1120R	100424
CR13,16	Diode, 1N4829	100443
F2	Fuse, 3 AG, .125 A	100592
F3	Fuse, 3 AG, 1 A Slow Blow	100584
Q1,3,4,7	Transistor, 2N3766	101373
Q2,6	Transistor, 2N2905	101382
Q5	Transistor, 40251	101354
R1	Resistor, 390 k, 1 W, ±5%, CC	101532
R2	Resistor, 220 k, 1/2 W, ±5%, CC	101458
R3,23	Resistor, 3.3 k, 1/4 W, ±5%, CC	10155901
R4,6,18	Resistor, 4.7 k, 1/2 W, ±5%, CC	101511
R5,19	Potentiometer, 5 k	101859
R7,8,13,22,29	Resistor, 1 k, 1/4 W, ±5%, CC	10156901
R9,14,30	Resistor, .68 Ω, 2 W, ±5%, WW	101829
R10,11,26,27	Resistor, 10 k, 1/8 W, ±1%, MF	106162
R12,28	Resistor, 4.7 k, 1/4 W, ±5%, CC	10159801
R15,20	Resistor, 1.5 k, 1/4 W, ±5%, CC	10157701
R16,17	Resistor, 1 k, 1 W, ±5%, CC	101635
R21	Resistor, 100 Ω, 1/4 W, ±5%, CC	10160901
R25	Resistor, 100 Ω, 1 W, ±5%, CC	101856
R31	Resistor, 330 Ω, 1 W, ±5%, CC	101624
R32,33	Resistor, 220 Ω, 1/4 W, ±5%, CC	10156601
R34,35	Resistor, 39 Ω, 1/4 W, ±5%, CC	10173301
U1,2	Integrated Circuit, 723PC	025761
U3	Integrated Circuit, 747PC	045205
W1	Wire, 24 AWG Solid Teflon	
XF2,3	Socket, Fuse (clip)	116299
XU1-3	Socket, 14-pin Augat	102433

PARTS LIST

POWER SUPPLY BOARD #041804-4-9 (Cont'd)

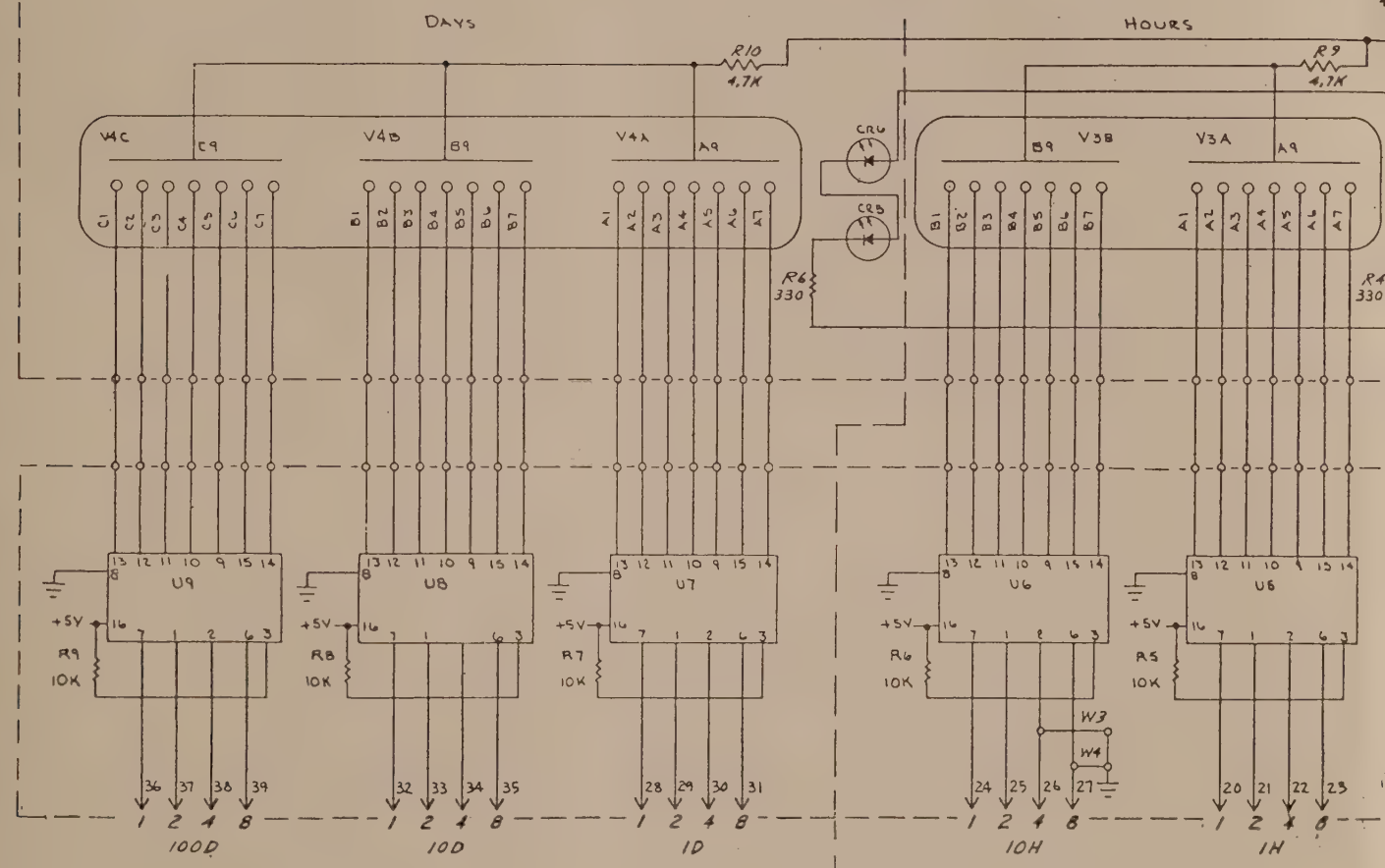
REFERENCE	DESCRIPTION	SD PART NO.
	Test Point, Red, +5 V	100541
	Test Point, Black, Grd.	100542
	Test Point, Green, -5 V	100543
	Test Point, Blue, +15 V	100547
	Test Point, Violet, -15 V	100548
	Socket, Pin	103037
	Heatsink	041805-1-1
	Pad, Transistor	100666
	Transistor, Modification	051124-1-1
	Angle, Front	041811-1-2
	Angle, Rear	041812-1-2
	Heatsink, Assembly	041805-4-1
	Solder, Wave	041804-3-9

CIRCUIT DESCRIPTION
DISPLAY ASSEMBLY
SCHEMATIC #041945-7 -2

1) GENERAL

The display assembly has one 3-digit and three 2-digit, in-line, planar indicator tubes and associated driver chips for the display of time in days, hours, minutes and seconds. LED colons are provided between the tubes. Time information is accepted in parallel BCD form. A voltage regulator is used to develop +180V from the +210V input for use by the display tubes.

The Assembly Drawing 041945-4-7 is formed from two main subassemblies plus the voltage regulator as shown on the schematic. The Readout Board Assembly 041766-4-1 mounts the display tubes and LED colons. The Driver Board Assembly 041772-4-1 mounts the display drivers which convert the BCD input to the 7-line required by the display tubes. The two boards are interconnected by right-angle pin assemblies.

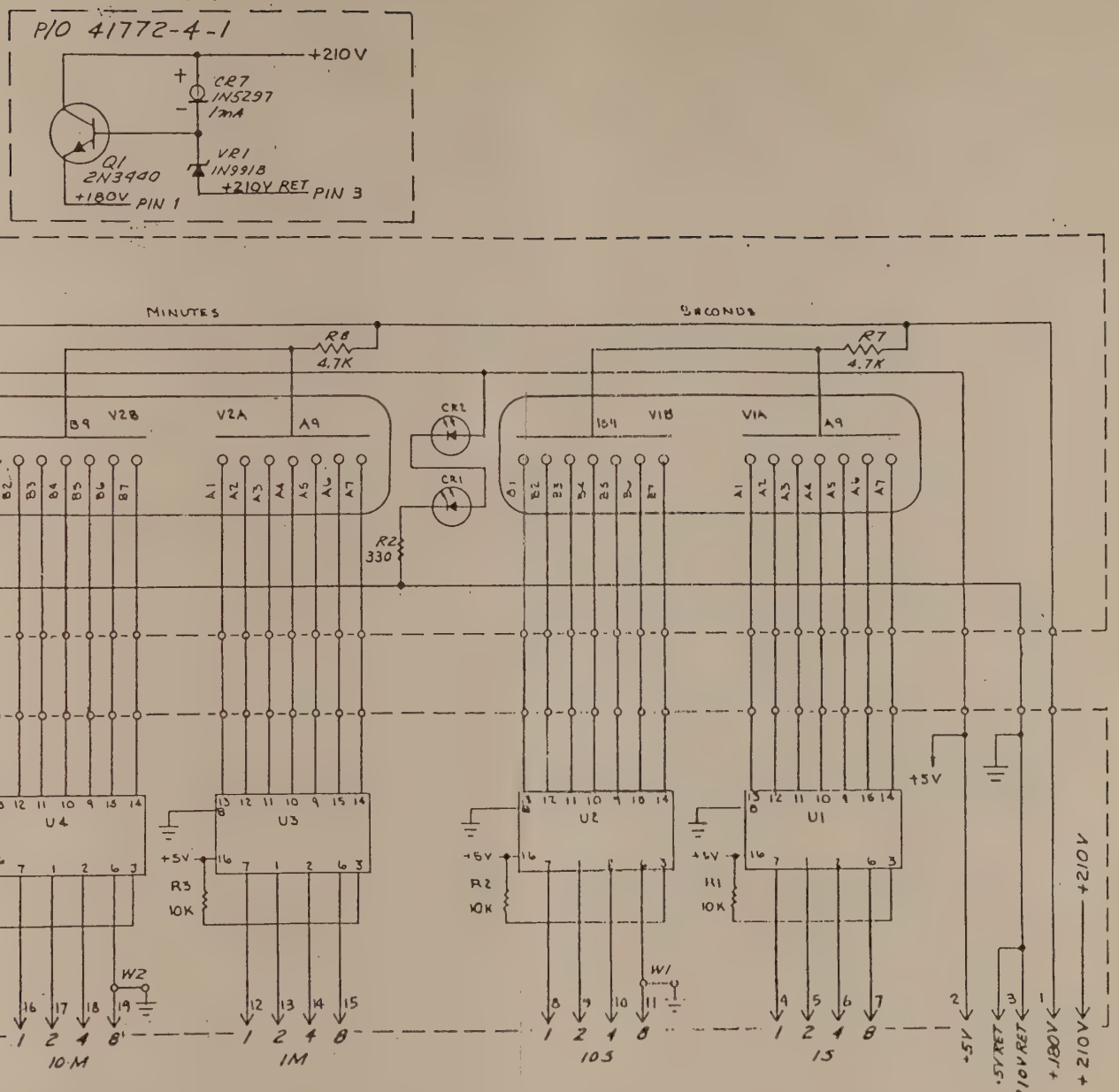


NOTE:
THIS SECTION NOT USED FOR UNITS WITHOUT DAYS

NOTES: (UNLESS OTHERWISE S

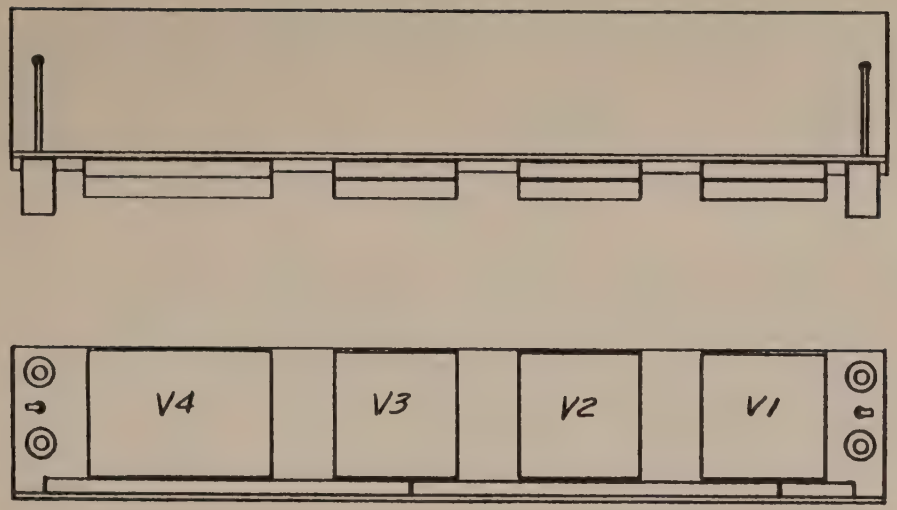
1. ALL RESISTORS ARE IN OHMS,
2. ALL DIODES ARE HP 5082-44
3. ALL IC's ARE DS8800N

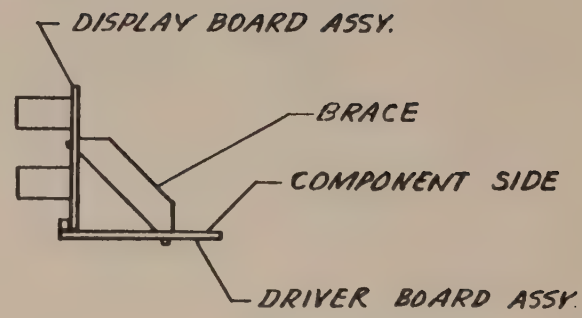
READ OUT AND DRIVER



CIFIED)
5%.

CHEMATIC #041945-7-2 REV H



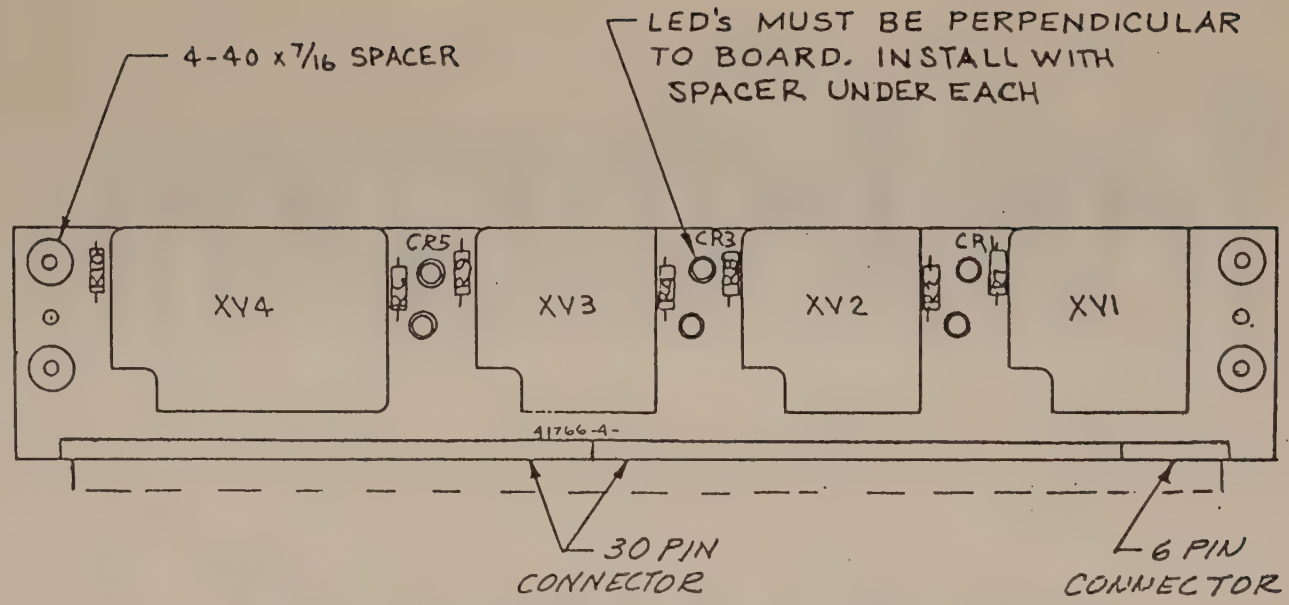


9 DIGIT DISPLAY ASSEMBLY #041945-4-7 REV B

PARTS LIST

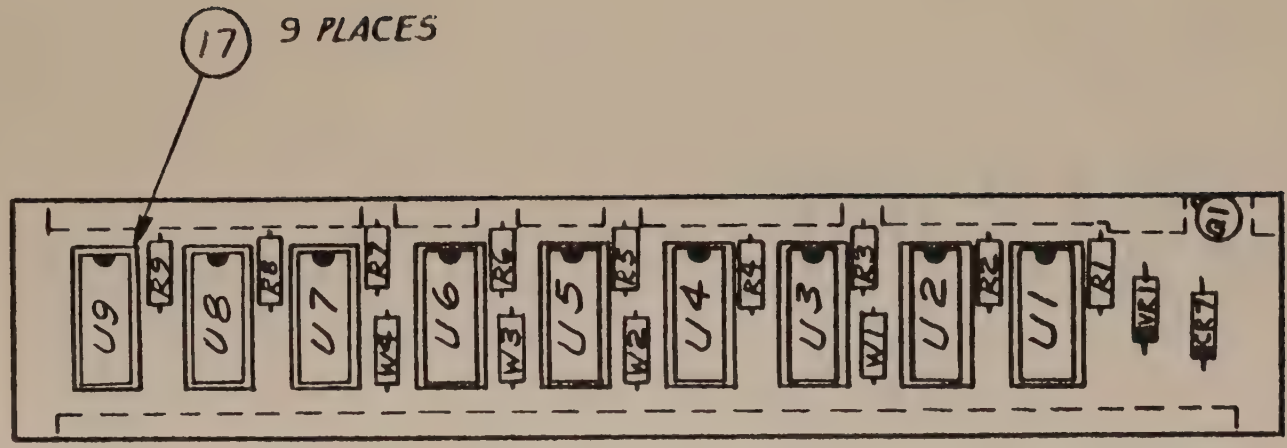
9 DIGIT DISPLAY ASSEMBLY #041945-4-7 REV C

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly, Display Board	041766-4-1
	Assembly, Display Driver	041772-4-1
	Schematic	041945-7-2
CR5,6	LED HP5082-4480	100460
U7,8,9	Integrated Ckt, DM8880N	045203
V1,2,3	Display Tube, SP352 Sperry	102403
V4	Display Tube, SP353 Sperry	102404
	Spacer LED	101077
	Bracket, Display & Driver	051450
	Driver Assembly Dwg.	041772-4-6



NOTE:
1.) CR 5 & 6 MOUNTED WITH DAYS OPTION ONLY.

9 DIGIT DISPLAY BOARD #041766-4-1 REV H



NOTE

1) DOTTED AREAS TO BE MASKED BEFORE FLOW SOLDERING.

9 DIGIT DISPLAY DRIVER BOARD #041772-4-6 REV B

PARTS LIST

DISPLAY ASSEMBLY #041766-4-1 REV H

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	041766-4-1
	Schematic	041945-7-2
CR1-4,6	Lamp, LED	100460
R2,4,6	Resistor, 120 Ω, 1/4 W, 5%	101536
R7-10	Resistor, 4.7 K, 1/4 W, 5%	101598
XV1-3	Socket, Display, 2 Digit	102445
XV4	Socket, Display, 3 Digit	102446
	Spacer, Swage	101062
	Connector, 30 pin Right Angle	101277
	Connector, Mod 6 pin	07189106

PARTS LIST

DISPLAY DRIVER ASSEMBLY #041772-4-1 REV H

REFERENCE	DESCRIPTION	SD PART NO.
	Assembly	041772-4-1
	Schematic	041945-7-2
CR7	Diode, 1N5297	100457
Q1	Transistor, 2N3440	101420
	Insulator	116544
R1-9	Resistor, 10 K, 1/4 W, 5%	101570
U1-9	Integrated Ckt, DM8880N	045203
VR1	Diode, Zener 180 V, 1N991B	100461
W1-4	Jumper, Molded	102879
XU1-9	Socket, 16 Pin	117041

CHAPTER SIX
STANDARD OPTIONS

1) GENERAL

A number of standard options are available for the Model 8132. Standard options, when supplied with the instrument, will be described on the following pages.

CIRCUIT DESCRIPTION
DAYS/ID (OPTION E13)
BLOCK DIAGRAM #7-061034

1) GENERAL

The Days/ID Option is shown on the instrument Block Diagram. This option adds the #21632-4-21 Days Accumulator Card (A18), Preset thumbwheel switches S12-S14, Leap Year/ID switch S16, a colon and three-digit display to Display Assembly (A102) and the associated wiring.

Parallel BCD Days/ID outputs are supplied to connector J3 through buffers on the Days Accumulator card. These 12-bits have the following specifications:

Code:	8-4-2-1.
Logic:	"1" = +5 ±0.5 V behind 6 kΩ.
	"0" = 0 +0.5 V, 12 mA sink.

All outputs are short-circuit-proof to ground.

An ID Update input (IC levels) to rear panel BNC connector J13, is provided. This input is fed to a circuit on the Modulator Board (A20).

PARTS LIST

DAYS/ID OPTION (E13) #06131602 REV B

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	061034
A18	Assembly, Days Accumulator	021632-4-21
CR5,6	Lamp, LED	100455
S33	Switch, Slide	102632
U7-9	Integrated Circuit, DD700	045203
V4	Display, SP353	102404
XA18	Connector, P.C.Edge	101204
	Card Guide	021340-1-2
	Eyelet (for S33)	112482
	DELETE	
S33	Cover Plate, Slide Switch	05120802

CIRCUIT DESCRIPTION
DAYS ACCUMULATOR
SCHEMATIC #021632-7-21

1) GENERAL

The Days Accumulator Card can provide up to 3 serial decades with common reset, parallel preset and 2 sets of buffered, parallel BCD outputs. Provision is made to gate one set of BCD outputs in three 4-bit bytes. The input may be either ac or dc-coupled and fed to the first decade through an update inhibit circuit. A days recycle circuit is included which may be programmed to reset the accumulator to 001 at the end of 365 or 366 days.

2) DECADE DIVIDERS

The up to 3 decade dividers are connected in tandum. Each is provided with parallel BCD data inputs which may be used to load preset information when the associated data strobe ($\overline{\text{PRESET}}$) line is grounded. The decade zero-reset inputs are wired in common through buffers on A8 to pin 23. The parallel BCD outputs from each decade are wired to output pins through 2 sets of buffers.

3) OUTPUT BUFFERS

The BCD output buffers may be inverting or noninverting. One of the 2 sets (A10, A13 and A15) can be gated by inputs through pins L,K and J, respectively. These gate lines are buffered by inverters A11.

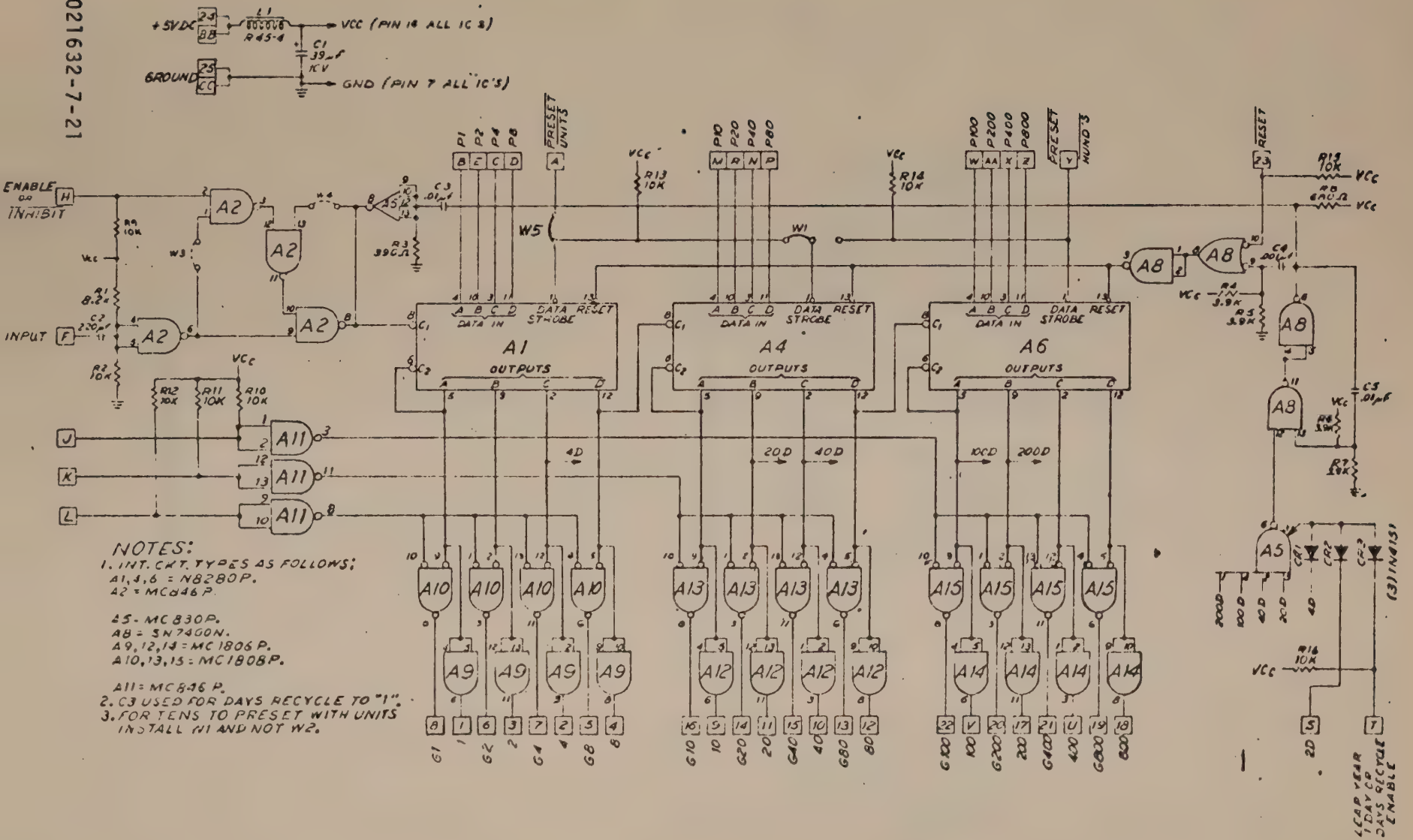
4) INPUT INHIBIT CIRCUIT

This circuit allows the presence of a ground on pin H to inhibit input signals on pin F from updating the accumulator. Gate A2-6 inverts and buffers the input. Gates A2-11 and A2-8 form an RS flip-flop.

A2-3 gates the $\overline{\text{INHIBIT}}$ line and the inverted input. When the accumulator is updating, flip-flop A2-8,11 output follows the input. When the $\overline{\text{INHIBIT}}$ line, pin H, is grounded, the flip-flop will latch with the output high. The output will go low the first time the input is low after the ground has been removed from the $\overline{\text{INHIBIT}}$ line.

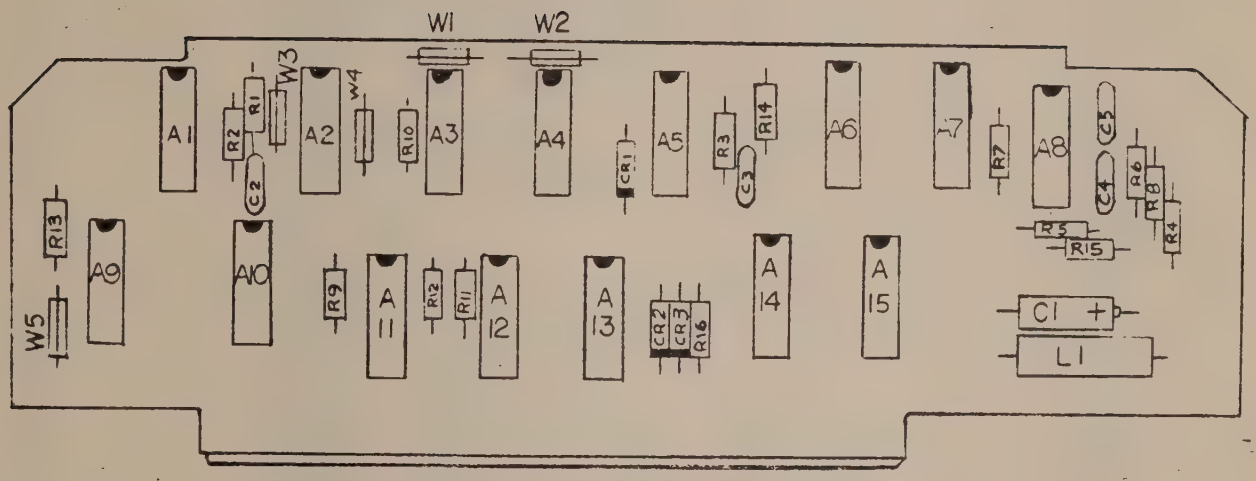
5) DAYS RECYCLE CIRCUIT

Gate 5-6 is a 4-input NAND gate with an expander input. The connection of diodes CR1-CR3 gives the gate 7-inputs. If recycle at 366 is desired, pin T is connected to Vcc. If recycle at 367 (for leap year) is desired, pin T is connected to pin 1 (the one day output). Pin S is always connected to the 2 day output. At the selected count, the output of A5-6 will go low, triggering one-shot A8-11,6. The one-shot output is a negative-going pulse (from +5 to 0 V). The leading edge of the pulse (ac-coupled into A8-8) causes the 3 dividers to reset to 000. The trailing edge of the pulse (which is positive-going) is ac-coupled into A5-8 where it is inverted and used to input 1 count to the first decade. The resulting accumulator contents are 001.



NOTES:
1. INT. CKT. TYPES AS FOLLOWS;
   A1, 4, 6 = N8280P.
   A2 = MC846P.
   A5 - MC830P.
   A8 = SN7400N.
   A9, 12, 14 = MC1806P.
   A10, 13, 15 = MC1808P.
   A11 = MC846P.
2. C3 USED FOR DAYS RECYCLE TO "1".
3. FOR TENS TO PRESET WITH UNITS INSTALL W1 AND NOT W2.

DAYS ACCUMULATOR SCHEMATIC #021632-7-21



DAYS ACCUMULATOR ASSEMBLY #021632-4-1 REV B

PARTS LIST

DAYS ACCUMULATOR #021632-7-21 REV A_n

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Assy. Dwg. #021632-4-1)	021632-4-21
	Schematic	021632-7-21
A1,4,6	Integrated Circuit, N8280P	025722
A2,11	Integrated Circuit, MC846P	019716
A5	Integrated Circuit, MC830P	019712
A8	Integrated Circuit, SN7400N	019705
A9,12,14	Integrated Circuit, MC1806P	025733
A10,13,15	Integrated Circuit, MC1808P	025734
C1	Capacitor, 39 µF, 10 V	100183
C2	Capacitor, 220 pF	100044
C3,5	Capacitor, .01 µF, Disc	100103
C4	Capacitor, .001 µF, Disc	100076
CR1-3	Diode, 1N4151	100385
L1	Inductor, R45-4	101313
R1	Resistor, 8.2 k 5%, 1/4 W	101595
R2,9-16	Resistor, 10 k 5%, 1/4 W	101570
R3	Resistor, 390 Ω 5%, 1/4 W	101592
R4-7	Resistor, 3.9 k 5%, 1/4 W	101601
R8	Resistor, 680 Ω 5%, 1/4 W	101669
W1,5	Jumper, Molded	102879
	Extractor	100865

CHAPTER SEVEN

SPECIAL MODIFICATIONS

1) GENERAL

Modifications to the Model 8132, requested by the customer, are documented in this chapter. These are usually extra-cost items to tailor the unit for a specific application.

CIRCUIT DESCRIPTION
TIME AND CONTROL BITS TO IEEE 488 BUS
BLOCK DIAGRAM #7-07160201

1) GENERAL

This option provides time or control bits on demand to the IEEE Bus as shown on Format Diagram #071611. Time data in days through seconds are presented in ASCII characters; most significant digit first. Colons are included between days and hours, hours and minutes and minutes and seconds. The group is terminated by carriage return and line feed characters. Control bits are presented as 10 8-bit bytes for a total of 80 bits. Separate device addresses are used to select time data and control bits.

2) CIRCUIT DESCRIPTION

Referring to the Block Diagram, IEEE Bus Control Cards A22, A23 and A24 provide the basic IEEE Bus Interface via J7. Rear panel Device Address switches S40 and S41 select the Time and Control addresses, respectively.

Parallel time data from the Accumulator are loaded into latches on Cards A26 and A27 which are normally in the follow mode. When time is demanded, the time in the latches is frozen and output onto the bus under the control of cards A22 and A23 plus circuits on Time Output Formatter A25.

Provision is included to initiate Service Requests at the start of each code frame.

The Controller on the Bus has access to time and control information at all times provided power is on and a code is being read.

Control bits are stored in two shift registers on Shift Register Card A7 under control of circuits on Bit Counter Card A20. The shift registers (A & B) store data from alternate code frames. When control bits are demanded, the contents of the idle shift register are dumped into a RAM on Data Distributor Card A21 under control of circuits on A20. The RAM contents are then loaded onto the bus in 8-bit bytes starting with the bits at the end of the code frame first (see Format). When the last of the 10 bytes are output on the bus the circuit will output null bytes (all bits zero) until Untalk is received or another talker is selected.

3) OPERATION

The interface, as used in this application, will obey the following Bus Commands:

IFC	Interface Clear
MLA	My Listen Address
MTA	My Talk Address
SPD	Serial Poll Disable
SPE	Serial Poll Enable
UNL	Unlisten
UNT	Untalk

The Service Request (SRQ) signal is asserted each code frame only if the unit has been designated a Listener or the SPE state exists. It is cleared when the unit is designated a Talker and the SPD message is sent. The SPE flip-flop is also cleared by IFC or pon.

CIRCUIT DESCRIPTION
TIME AND CONTROL BITS TO IEEE 488 BUS
BLOCK DIAGRAM #7-07160201

1) GENERAL

This option provides time or control bits on demand to the IEEE Bus as shown on Format Diagram #071611. Time data in days through seconds are presented in ASCII characters; most significant digit first. Colons are included between days and hours, hours and minutes and minutes and seconds. The group is terminated by carriage return and line feed characters. Control bits are presented as 11 8-bit bytes for a total of 88 bits. Separate device addresses are used to select time data and control bits.

2) CIRCUIT DESCRIPTION

Referring to the Block Diagram, IEEE Bus Control Cards A22, A23 and A24 provide the basic IEEE Bus Interface via J7. Rear panel Device Address switches S40 and S41 select the Time and Control addresses, respectively.

Parallel time data from the Accumulator are loaded into latches on Cards A26 and A27 which are normally in the follow mode. When time is demanded, the time in the latches is frozen and output onto the bus under the control of cards A22 and A23 plus circuits on Time Output Formatter A25.

Provision is included to initiate Service Requests at the start of each code frame.

The Controller on the Bus has access to time and control information at all times provided power is on and a code is being read.

Control bits are stored in two shift registers on Shift Register Card A7 under control of circuits on Bit Counter Card A20. The shift registers (A & B) store data from alternate code frames. When control bits are demanded, the contents of the idle shift register are dumped into a RAM on Data Distributor Card A21 under control of circuits on A20. The RAM contents are then loaded onto the bus in 8-bit bytes starting with the bits at the end of the code frame first (see Format). When the last of the 11 bytes are output on the bus the circuit will output null bytes (all bits zero) until Untalk is received or another talker is selected.

3) OPERATION

The interface, as used in this application, will obey the following Bus Commands:

IFC	Interface Clear
MLA	My Listen Address
MTA	My Talk Address
SPD	Serial Poll Disable
SPE	Serial Poll Enable
UNL	Unlisten
UNT	Untalk

The Service Request (SRQ) signal is asserted each code frame only if the unit has been designated a Listener or the SPE state exists. It is cleared when the unit is designated a Talker and the SPD message is sent. The SPE flip-flop is also cleared by IFC or pon.

REVISIONS					
REV	DESCRIPTION	ECR NO	ECO NO	DATE	APP BY
B	RELEASED TO RECORDS			4/71	

BIT →	7	6	5	4	3	2	1	0	
DIO →	8	7	6	5	4	3	2	1	BYTE ↓
	98	97	96	95	93	92	91	90	#10
	88	87	86	85	83	82	81	80	#9
	78	77	76	75	73	72	71	70	#8
	68	67	66	65	63	62	61	60	#7
	58	57	56	55	53	52	51	50	#6
	48 / Ø	47 / Ø	46 / Ø	45 / Ø	43 / 600D	42 / 400D	41 / 200D	40 / 100D	#5
	38 / 80D	37 / 40D	36 / 20D	35 / 10D	33 / 8D	32 / 4D	31 / 2D	30 / 1D	#4
	28 / Ø	27 / Ø	26 / 20H	25 / 10H	23 / 8H	22 / 4H	21 / 2H	20 / 1H	#3
	18 / Ø	17 / 40M	16 / 20M	15 / 10M	13 / 8M	12 / 4M	11 / 2M	10 / 1M	#2
	8 / 40S	7 / 20S	6 / 10S	5 / Ø	4 / 8S	3 / 4S	2 / 2S	1 / 1S	#1

CLASS II FORMAT

NOTES: (CLASS II)

1. THE NUMBERS IN THE CHART REFER TO THE X,Y ADDRESS OF THE DESIGNATED BITS IN THE TIME CODE FRAME FOR EXAMPLE: 98 = Y9, X8.
2. BYTES #1 THRU #5 CONTAIN TIME DATA IN SECONDS THRU DAYS IN THE TIME CODE PLUS LOGGING DATA FORMAT. BITS "Ø" ARE ALWAYS ZERO IN THIS FORMAT.
3. BIT LOCATIONS 99, 94, 89, 84, 79, 74, 69, 64, 59, 54, 49, 44, 39, 34, 29, 24, 19, 14, 09 AND 00 ARE IGNORED.

LIST OF MATERIALS

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	NOMENCLATURE OR MFG NO

DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SYSTRON DONNER CORPORATION CONCORD CALIFORNIA
CHECK	DATE	DECIMAL TOLERANCE .X ±.1 .XX ±.03 ANGLES ±	CODE IDENT 53947
ELECT	DATE		
MECH	DATE		
QA			
SCALE		DO NOT SCALE DRAWING	MATERIAL

CLASS II FORMAT

DRAWING NO. — PART NO. — REV

PROPRIETARY DATA

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REVISIONS					
REV	DESCRIPTION	SER NO	ECO NO	DATE	APP'D BY
A	RELEASED TO RECORDS			9/76	
B	REVISED	—	—	9/77	

Character	
#1	HUNDREDS DAYS
#2	TENS DAYS
#3	UNITS DAYS
#4	COLON
#5	TENS HOURS
#6	UNITS HOURS
#7	COLON
#8	TENS MINUTES
#9	UNITS MINUTES
#10	COLON
#11	TENS SECONDS
#12	UNITS SECONDS
#13	CARRIAGE RETURN
#14	LINE FEED

CLASS I FORMAT

NOTES:

1. Time Data are sent in ASCII Format, Character #1 first.
2. An Interrupt is generated at the start of each Time Code frame if the device has been designated a listener.

LIST OF MATERIALS

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

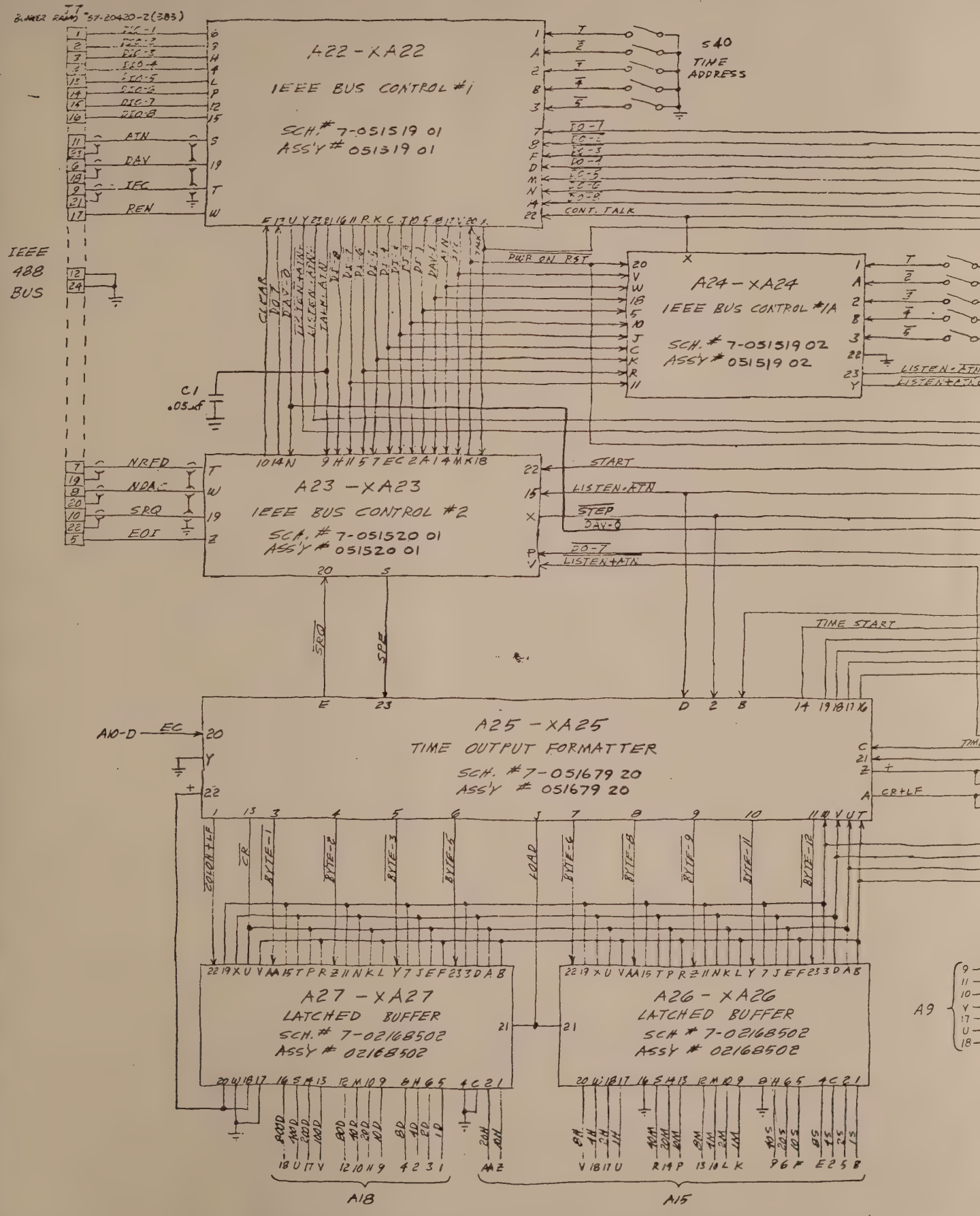
PROPRIETARY DATA
Provided under United States Government Contract No. _____
Shall not be either released outside the Government, or used, duplicated, or disclosed in whole or in part for manufacture or procurement, without the written permission of Syntron Division Donner Corporation except for (1) emergency repair or overhaul work by or for the Government, where the item or process concerned is not otherwise restrictively controlled to ensure timely performance of the work, or (2) release to a foreign government, as the interests of the United States may require, provided that proper steps for the control and disposition of the proprietary data will be taken in the foreign jurisdictions. This legend shall be marked on any reproduction hereof in whole or in part.

DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .x ±.0 .xx ±.03 ANGLES ±	SYNTRON DONNER CORPORATION CONCORD CALIFORNIA
CHECK	DATE		
E.I.C.T.	DATE		CODE IDENT 53947
[illegible]	DATE		
[illegible]	DATE		
QA	DATE		
1 SEQ ON / NEXT ASSY	SCALE	DO NOT SCALE DRAWING	MATERIAL
APPLICATION		SH 1 OF 2	

CLASS I FORMAT

DRAWING NO. 71C-11 REV B

B1


A22 - XA22
IEEE BUS CONTROL #1
SCH.# 7-051519 01
ASS'Y # 051519 01
S40
TIME ADDRESS
CONT. TALK
IEEE 488 BUS
ATN
DAV
IFC
REN
NRFD
NDAC
SRQ
EOI
C1
.05 uf
A24 - XA24
IEEE BUS CONTROL #1A
SCH. # 7-051519 02
ASS'Y # 051519 02
PWR ON RST
CLEAR
DAV-2
LISTEN+ATN
LISTEN+ATN
A23 - XA23
IEEE BUS CONTROL #2
SCH. # 7-051520 01
ASS'Y # 051520 01
START
LISTEN+ATN
STEP
DAV-0
DO-7
LISTEN+ATN
SRQ
SPE
TIME START
A25 - XA25
TIME OUTPUT FORMATTER
SCH. # 7-051679 20
ASS'Y # 051679 20
A10-D
EC
CR+LF
LOAD
BYTE-1
BYTE-2
BYTE-3
BYTE-5
BYTE-6
BYTE-8
BYTE-9
BYTE-11
BYTE-12
A27 - XA27
LATCHED BUFFER
SCH. # 7-02168502
ASS'Y # 02168502
A26 - XA26
LATCHED BUFFER
SCH # 7-02168502
ASS'Y # 02168502
A9
A18
A15

REVISIONS				
LTR	DESCRIPTION	ENG ORD NO	MFG ORD NO	DATE
A	RELEASE TO RECORDS	—	—	5-1-74
B	ADDED A21-17 TO A21-22	—	—	6-4-74
C	ADDED A6	—	—	6-11-74

NOTES:
1. THE CIRCUITRY SHOWN IS SUPERIMPOSED ON THE BASIC UNIT BLOCK DIAGRAM.
2. GROUND IS CONNECTED TO PINS 25 & CC AND +5V TO PINS 24 & BB ON ALL CARDS.
3. THE ADDRESS SWITCHES S40 & S41 ARE MOUNTED ON THE REAR PANEL.
4. DAYS OPTION E13 MUST BE INSTALLED.

S41 CONTROL ADDRESS

A20 – XA20
BIT COUNTER
SCH. # 7-051679 21
ASS'Y # 051679 21

A21 – XA21
DATA DISTRIBUTOR
SCH. # 7-051679 22
ASS'Y # 051679 22

A7 – XA7
SHIFT REGISTER
SCH. # 7-051679 23
ASS'Y # 05167923

X6 – XA6
UNIVERSAL LOGIC
SCH # 7-05164555

WRITE
DN
LOAD
TRIGGER
GATED CLOCK
DATA
SERIAL ONES
TPPS
A12-K
A12-15
A12-R
A9
0.01S
0.08S
0.1S
0.8S
SHIFT
SEL A
SEL B
PUMP A
PUMP B
GATE
CLOCK
X9
X9 • X4 • Y0

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

PROPRIETARY DATA
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DRAWN	DATE	UNLESS OTHERWISE SPECIFIED / DIMENSIONS ARE IN INCHES	SYSTRON DONNER CORPORATION, CONCORD, CALIFORNIA
CHECK	DATE	DECIMAL TOLERANCE .X ±.XX ±.XXX ANGLES ±	CODE IDENT. 53947
ELECT.	DATE		
MECH.	DATE		
PROJECT.	DATE		
QA	DATE		
USED ON	NEXT ASSY	SCALE	DO NOT SCALE DRAWING
APPLICATION			SH / OF /

TIME OF CONTROL BITS TO IEEE 488 BUS

MATERIAL

DRAWING NO. REF	SIZE	PART NO.	REV.
7	D	07160201	C

PARTS LIST

TIME AND CONTROL BITS TO IEEE 488 BUS #07160201 REV B

REF.	DESCRIPTION	SD PART NO.
	ADD	
	Schematic	7-07160201
	Format Drawing	071611
A1	Assembly, Extender	021507-4-1
A6	Assembly, Universal Logic	05164555
A7	Assembly, Shift Register	05167923
A20	Assembly, Bit Counter	05167921
A21	Assembly, Data Distributor	05167922
A22	Assembly, IEEE Bus Control #1	05151901
A23	Assembly, IEEE Bus Control #2	05152001
A24	Assembly, IEEE Bus Control #1A	05151902
A25	Assembly, Time Output Format	05167920
A26,27	Assembly, Latched Buffer	02168502
J7	Connector, 24 pin	117054
	Connector Adapter	05192503
S40,41	Switch (Molex #A-10040-107)	
XS40,41	Socket (Augat #314-AG6A-3R)	
XA1,6,7,20,22-27	Connector, PC Edge	101204
	Mod. Osc. Cover Plate	05191310
(J7)	Standoff	057361
	Spacer (#2 .437L x .125 O.D.)	116235

* * * * * * * * * *

DELETE

A21	Assembly, Extender	021507-4-1
J7	Cover Plate, 36 pin	031124-1-1
	Cover Plate, Osc.	05191310

CIRCUIT DESCRIPTION
LATCHED BUFFER
SCHEMATIC #7-02168502

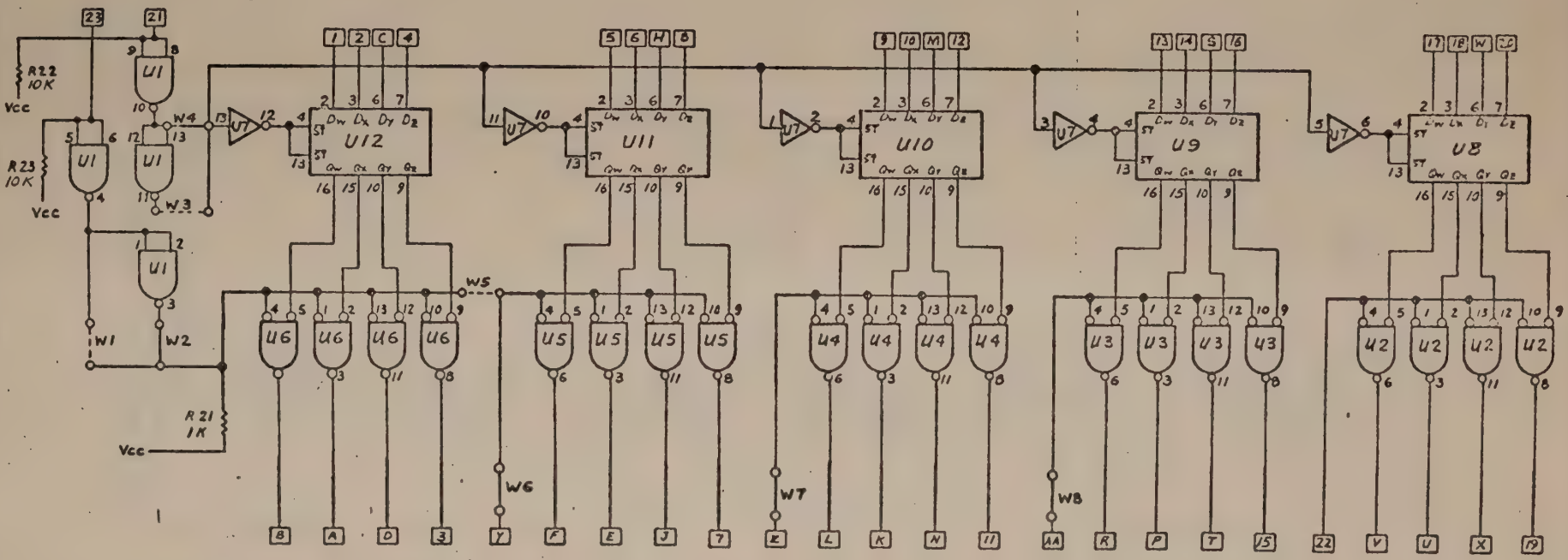
1) GENERAL

This card contains five quad-latches and 20 non-inverting buffers.

2) FUNCTION

Each of the latches (U8-U12) has the property that a signal applied to a to a "D" input is transferred to the corresponding "Q" output when the $\overline{ST}$ input is high, i.e. "Q" will copy "D" when $\overline{ST}$ is high. The "Q" output retains its last state when $\overline{ST}$ is low. The $\overline{ST}$ inputs are controlled via pin 21, U1-10 and inverters on U7.

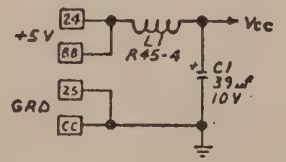
The output buffers on U2-U6 gate the contents of the latches onto the associated output lines. These buffers are controlled in groups of four via pins 23, Y, Z, AA and 22.



NOTE: UNLESS OTHERWISE SPECIFIED

1. RESISTORS: 10 KΩ, ¼ W, C.C.

3. I.C. MC857P - U1.
   " MC1808P - U2, U3, U4, U5 & U6.
   " SN7404N - U7.
   PIN 7 IS CONNECTED TO GRD.
   PIN 14 " " " Vcc.
4. I.C. SN7475N - U8, U9, U10, U11 & U12
   PIN 12 IS CONNECTED TO GRD.
   PIN 5 " " " Vcc.

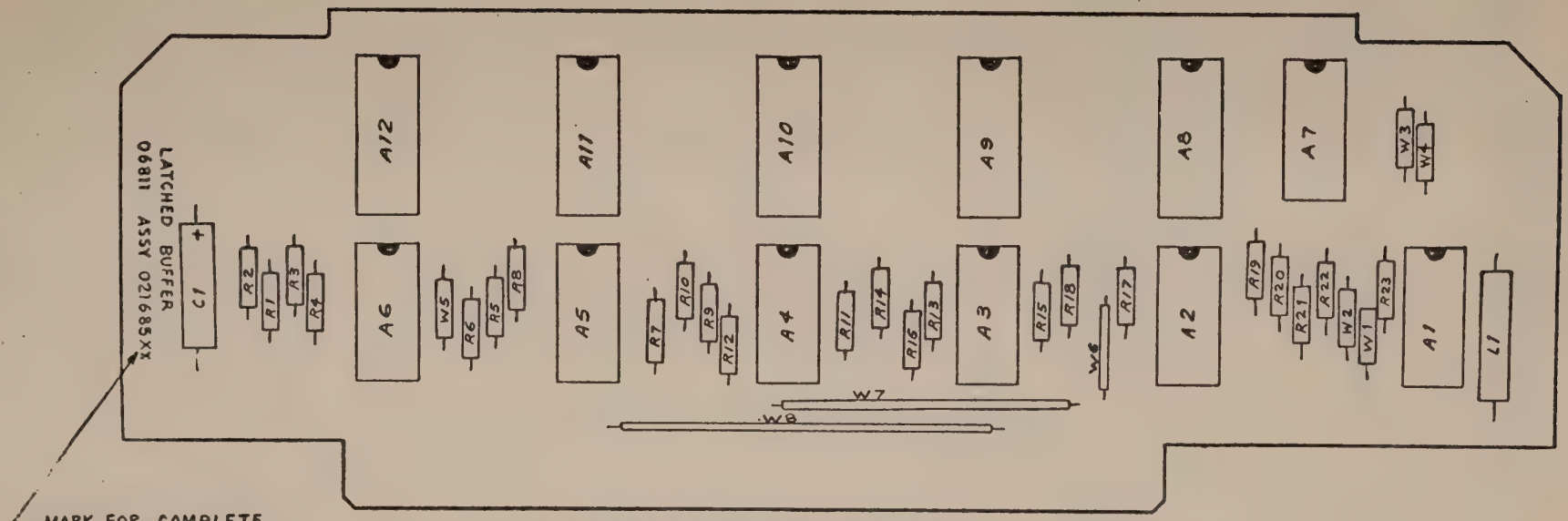


PROPRIETARY DATA

CORPORATION
CONCORD CALIFORNIA
CODE IDENT 06011

LATCHED BUFFER

7 02167-5-07



REVISIONS					
NONE	DESCRIPTION				

SYSTRON DONNER CORPORATION
CONCORD, CALIFORNIA
CODE IDENT 06811

LATCHED BUFFER

PARTS LIST

LATCHED BUFFER ASSEMBLY #7-02168502 REV A_1

REF.	DESCRIPTION	SD PART NO.
	Assembly (Ref. Assy. Dwg. #02168501)	02168502
	Schematic	7-02168502
C1	Capacitor, 39 µF, 10 V	100183
L1	Inductor, R45-4	101313
R21	Resistor, 1 k 5%, 1/4 W	101569
R22,23	Resistor, 10 k 5%, 1/4 W	101570
U1	Integrated Circuit, MC857P	025753
U2-6	Integrated Circuit, MC1808P	025734
U7	Integrated Circuit, SN7404N	025779
U8-12	Integrated Circuit, SN7475N	045201
W2,4	Jumper, Molded	102879
	Extractor	100865

CIRCUIT DESCRIPTION
IEEE BUS CONTROL
SCHEMATICS #7-05151901 & #7-05152001

1) GENERAL

The basic IEEE Bus Interface is contained on two cards, IEEE Bus Control #1 and #2. These cards contain circuitry essential for communications over the bus as required by IEEE Std. 488-1975.

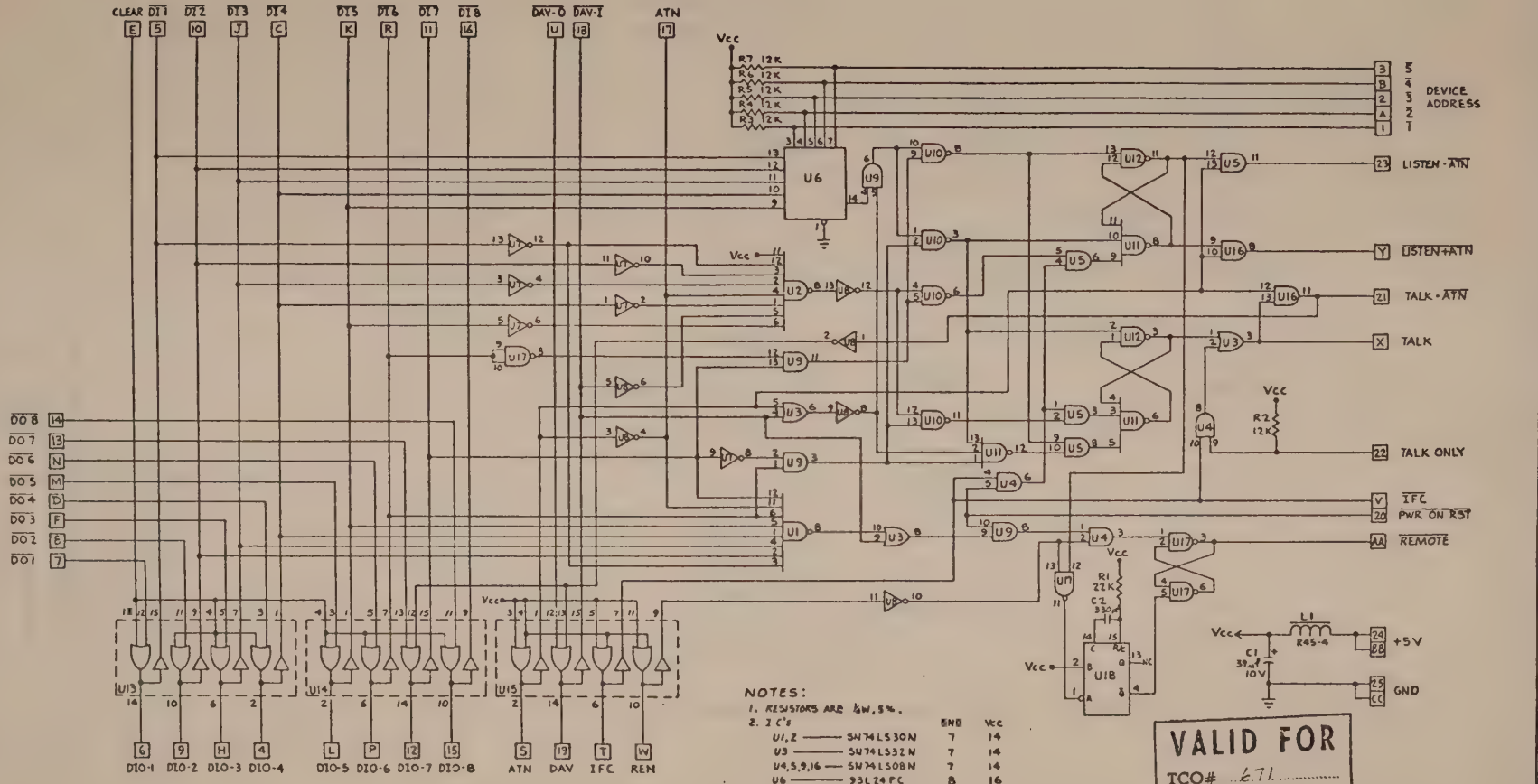
2) CIRCUIT DESCRIPTION

The IEEE Bus Control #1 card contains drivers and receivers on chips U13, U14 and U15 for the eight Data Bus lines (DIO 1-8) plus the Data Valid (DAV), Interface Clear (IFC), Attention (ATN) and Remote Enable (REN) control lines. The drivers are enabled only when the device is designated a Talker. Comparator chip U6 responds when the Device Address selected on external switches appears on the Data Bus. The remaining gates on the card decode and react to the following multiline interface messages: Go To Local (GTL), My Listen Address (MLA), My Talk Address (MTA), Unlisten (UNL) and Untalk (UNT). Flip-flop U12-11/U11-8 or U12-3/U11-6 is set when the device is designated a Listener or a Talker, respectively. Each flip-flop is cleared when the other is set. The Talk flip-flop is also cleared if any other device on the bus is designated a Talker. Both flip-flops are cleared by IFC or Power On Reset (pon). Flip-flop U17-6/3 is set when the REN line is first asserted enabling remote control of the device. It is cleared by REN going false or by GTL or pon.

The IEEE Bus Control #2 card contains drivers and receivers on chips U16 and U17 for the Service Request (SRQ), End or Identify (EOI), Not Ready for Data (NRFD) and Not Data Accepted (NDAC) control lines. The NRFD and NDAC drivers are enabled only when ATN is true or when the device is designated a Listener. In these modes the acceptor handshake is provided by one-shots on U12 and flip-flops on U6. One-shot U12-4 provides a delay before assertion of NRFD at U6-6. One-shot U12-5 develops a strobe through gates on U8, U9 and U15 for the loading of data. It sets NDAC flip-flop U6-9 high on the trailing edge.

When the device is designated a Talker the source handshake is provided by one-shots on U5 and U11 plus flip-flops on U10 and U15. Flip flop U15-6/3 is set by U11-12 output when NRFD is high and a data byte is stable on the Data Bus lines driving the DAV line low through a driver on Control #1 card. It is cleared by U10-8 after a delay through U5-4 when the NDAC line goes high. It is clamped in clear when Talk is cleared. One-shots U5-12 and U11-4, flip-flop U10-5 plus gates U4-3 and U8-8 form a sequencer used to control the loading of data bytes onto the Data Bus.

A Service Request (SRQ) may be initiated by asserting the SRQ line through a driver on U16. Circuitry is included to provide the appropriate response to a Serial Poll from the bus controller. Flip-flop U2-11/8 is set whenever the Serial Poll Enable (SPE) multiline interface message is detected by decoder U7-8/U1-6. The output from U2-8 drives the DIO-7 Data Bus line low through U4-11, U9-4 and a driver on Control #1 card provided the device is designated a Talker and SRQ is asserted. The U2-11/8 flip-flop is cleared by the Serial Pole Disable (SPD) multiline message via U7-8/U1-3 or by pon or IFC.



NOTES:

1. RESISTORS ARE ¼W, 5%.
2. I C's

		GND	Vcc
U1,2	SN74LS30N	7	14
U3	SN74LS32N	7	14
U4,5,9,16	SN74LS08N	7	14
U6	93L24PC	8	16
U7,8	SN74LS04N	7	14
U10,12,17	SN74LS00N	7	14
U11	SN74LS10N	7	14
U13,14,15	MC3446P	8	16
U18	SN74LS123N	8	16

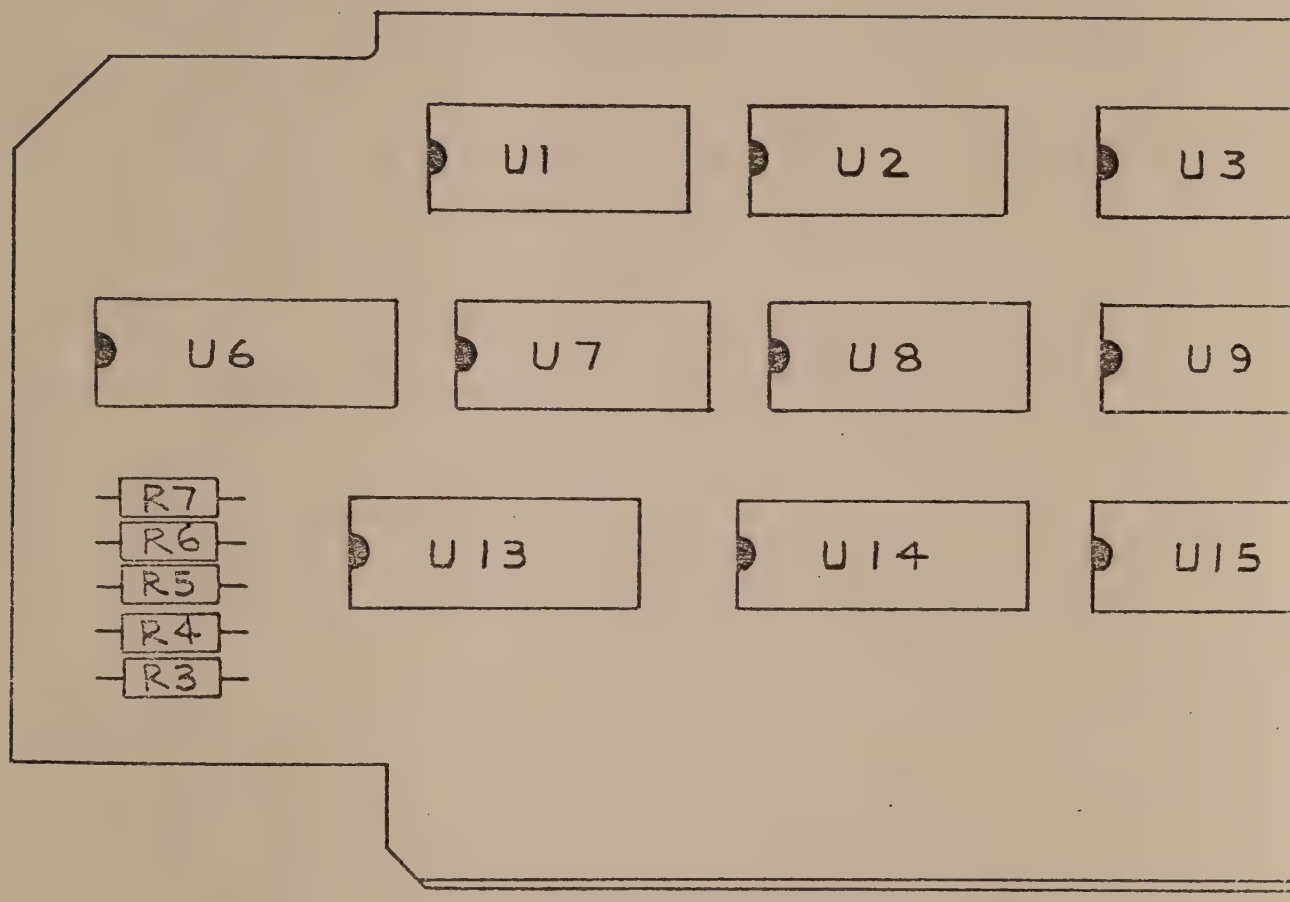
VALID FOR TCO# 671 ONLY

LIST OF MATERIALS

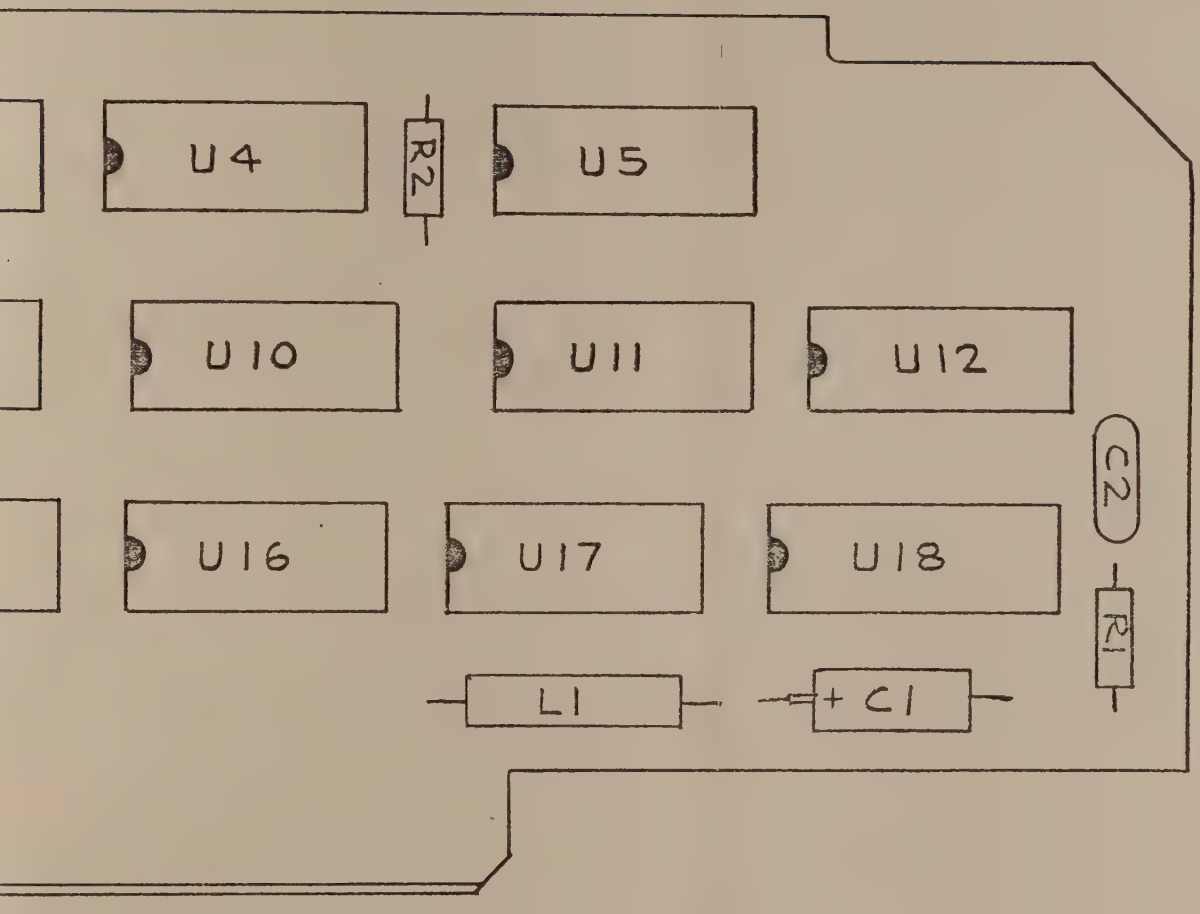
SCHEMATIC, IEEE BUS CONTROL #1 PC BOARD

CODE IDENT 53947

7 D 051519 01 A


U1
U2
U3
U6
U7
U8
U9
R7
R6
R5
R4
R3
U13
U14
U15

REVISIONS					
REV	DESCRIPTION	SER NO	ECO NO	DATE	APP BY
A	RELEASED TO RECORDS			7/3/	
B	SHT. 2 REDRAWN (NEW A/N).	—	11403	3/19/	



ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

PROPRIETARY DATA

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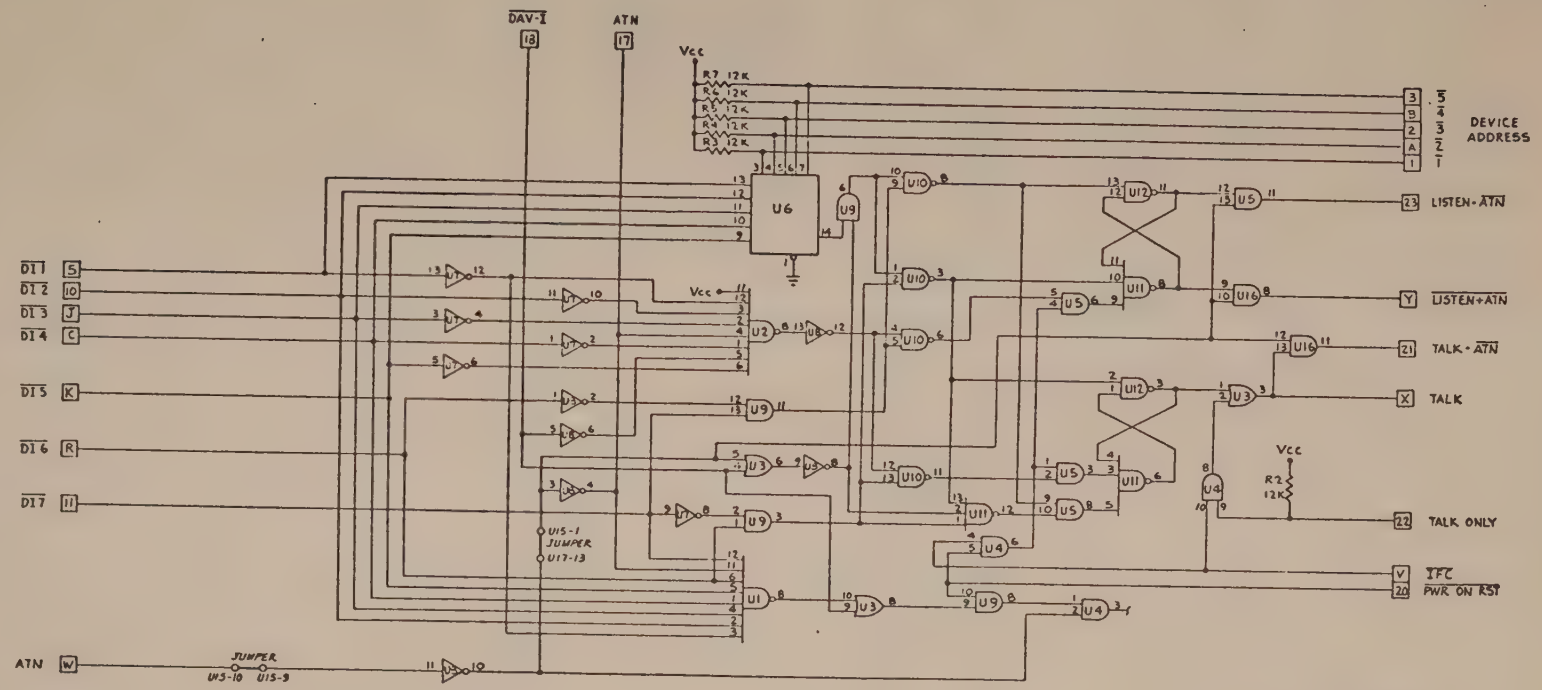
		DRAWN BILL 07/29/70 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ± .XX ± .XXX ± ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	P.C.BOASSY, IEEE BUS CONTROL № 1
		CHECK DATE			
		ELECT. DATE			
		MECH DATE			
8155-0424		PROJECT DATE		CODE IDENT 53947	
8132-0151		QA DATE			
USED ON	NEXT ASSY	SCALE 2/1	DO NOT SCALE DRAWING	MATERIAL	DRAWING NO. REF: B SIZE: SIZE PART NO.: 05151901 REV: B
APPLICATION			SH 1 OF 2		

PARTS LIST

P.C. BOARD ASSEMBLY, IEEE BUS CONTROL #1 #05151901 REV A

REF.	DESCRIPTION	SD PART NO.	
	Assembly	05151901	
	Schematic	7-05151901	
C1	Capacitor, 39 µF, 10 V	100183	
C2	Capacitor, 330 pF, DM	100276	
L1	Inductor, R45-4	101313	
R1	Resistor, 22 k, ¼ W	101572	
R2-7	Resistor, 12 k, ¼ W	101565	
U1,2	Integrated Circuit, SN74LS30N	103971	
U3	Integrated Circuit, SN74LS32N	103972	
U4,5,9,16	Integrated Circuit, SN74LS08N	103967	
U6	Integrated Circuit, 93L24PC	117020	
U7,8	Integrated Circuit, SN74LS04N	103749	
U10,12,17	Integrated Circuit, SN74LS00N	103130	
U11	Integrated Circuit, SN74LS10N	103968	
U13,15	Integrated Circuit, MC3446	117021	11702
U18	Integrated Circuit, SN74LS123N	103976	
	Extractor	100865	



NOTES :

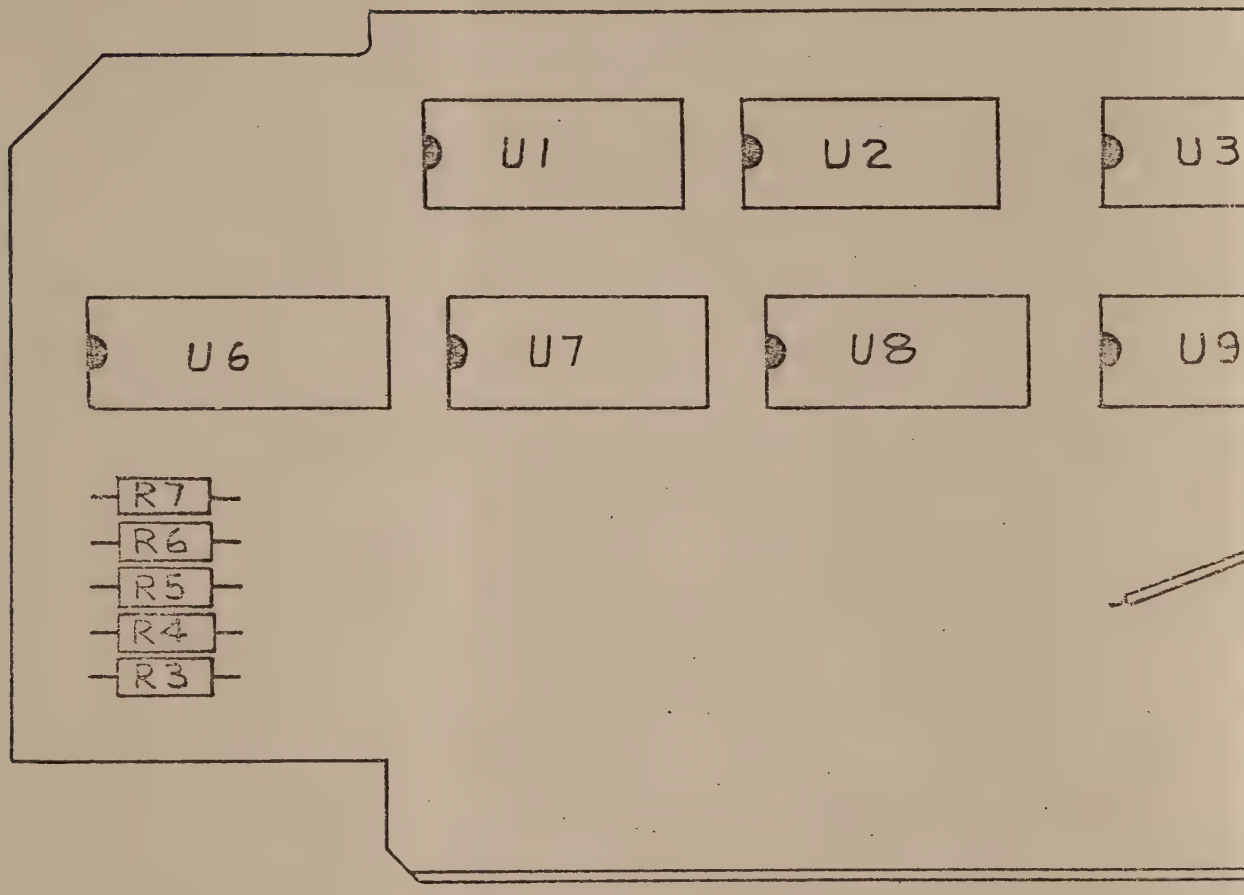
1. RESISTORS ARE ¼W, 5%.
2. IC's

		GND	Vcc
U1,2	SN74LS30N	7	14
U3	SN74LS32N	7	14
U4,5,9,16	SN74LS08N	7	14
U6	93L24PC	8	16
U7,8	SN74LS04N	7	14
U10,12	SN74LS00N	7	14
U11	SN74LS10N	7	14

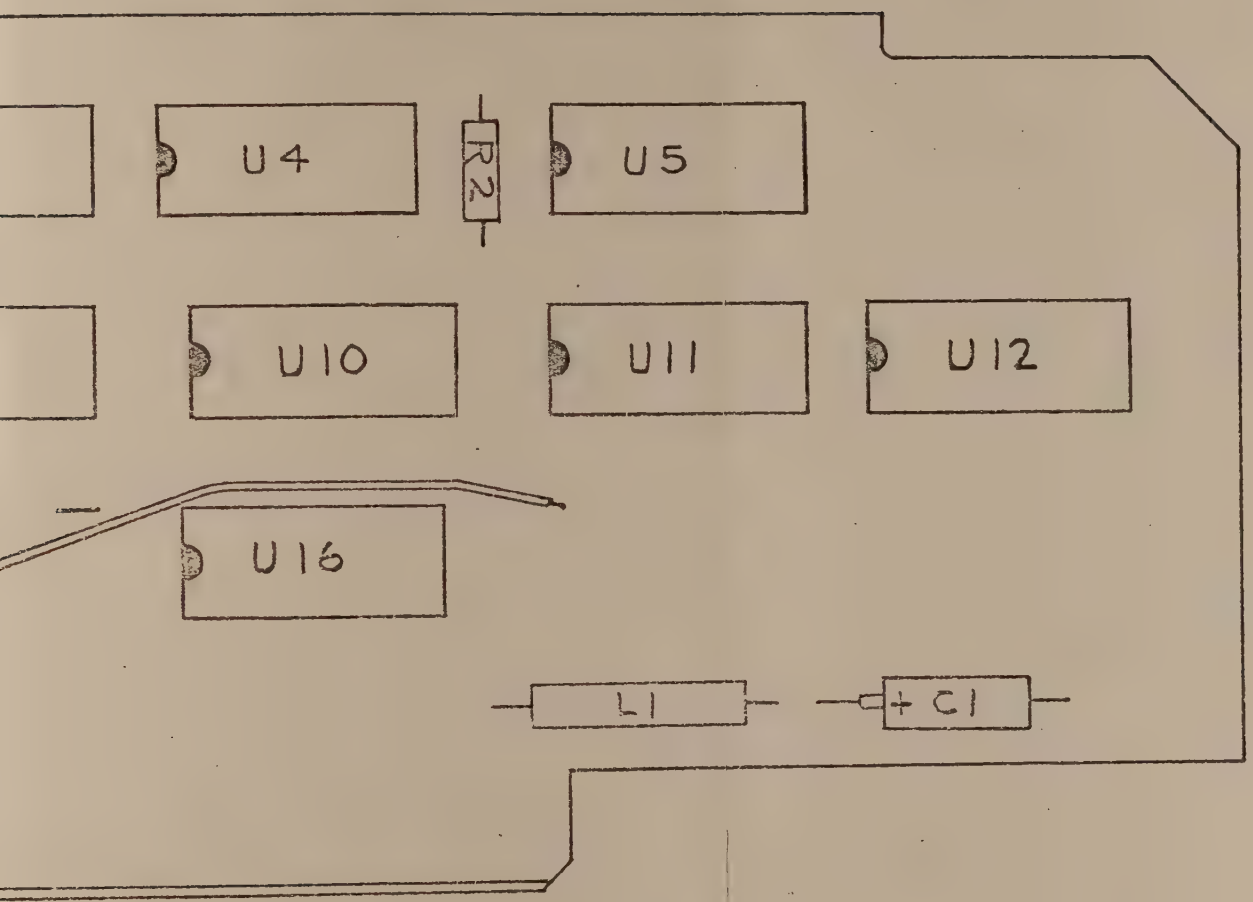
VALID FOR TCO# 671 ONLY

LIST OF MATERIALS

CODE IDENT 53947	SCHEMATIC, IEEE BUS CONTROL = 1A P.C. BOARD
7 D	05151902 A


U1
U2
U3
U6
U7
U8
U9
R7
R6
R5
R4
R3

REVISIONS				
REV	DESCRIPTION	NO.	DATE	
A	RELEASED TO RECORDS			
B	SHT. 2 REDRAWN (NEW A/W).	—	11405	



ITEM NO	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

PROPRIETARY DATA

Furnished under United States Government Contract No. _____
Shall not be either released outside the Government, or used, duplicated, or disclosed in whole or in part for manufacture or procurement, without the written permission of Systron-Donner Corporation except for (1) emergency repair or overhaul work by or for the Government where the item or process concerned is not otherwise reasonably available to enable timely performance of the work, or (2) release to a foreign government, as the interests of the United States may require, provided that in either case the release use, duplication or disclosure hereof shall be subject to the foregoing limitations. This legend shall be marked on any reproduction hereof in whole or in part

DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X .XX .XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA
CHECK	DATE		
ELECT.	DATE		
MECH.	DATE		
PROJECT	DATE		
QA	DATE		

CODE IDENT 53947

P.C.BD. ASSY., IEEE BUS CONTROL #1A

USED ON	NEXT ASSY
APPLICATION	

SCALE 2/1 | DO NOT SCALE DRAWING | SH 1 OF 2

MATERIAL

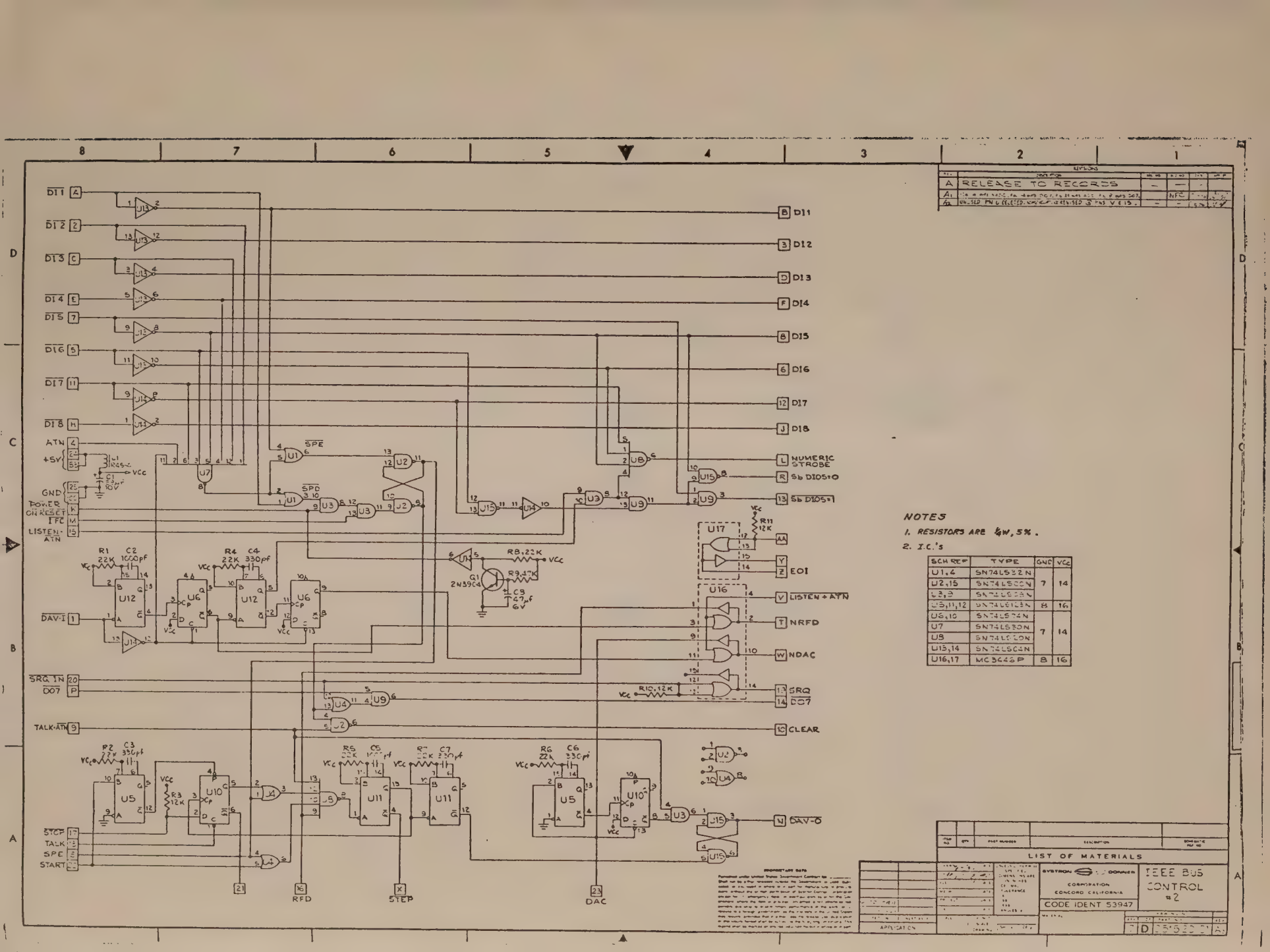
DRAWING NO.			REV
REF	SIZE	PART NO.	
	B	05151902	B

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
1	B	0515 1902	P.C. ASSY.		X			
2			SCHEMATIC	7DC0515 1902	Ref			
3	B	C515 19	P.C. BOARD		1			
4			P.C. BOARD ARTWORK	2DC0515 19	Ref			
6		100865	EXTRACTOR		2			
7		101313	INDUCTOR R45-4	L1	1			
9		100123	CAPACITOR, 39 µf, 10 V	C1	1			
11		101565	RESISTOR, 12K, ¼W	R2	5			
12				R3 S/A R2				
13				R4				
14				R5				
15				R6				
16				R7				
18			24 GA. BARE BUS		Ref			
19			24 GA. INSULATED BUS		Ref			
21		103971	INT. CKT. SN74LS30N	U1	2			
22				U2 S/A U1				
23		103972	SN74LS32N	U3	1			
24		103967	SN74LS08N	U4	4			
25				U5 S/A U4				
26		117029	93L24PC	U6	1			
27		105719	SN74LS04N	U7	2			
28				U8 S/A U7				
29				U9 S/A U4				
30		103130	SN74LS00N	U10	2			
31		103959	SN74LS10N	U11	1			
32				U12 S/A U10				
33				U13 S/A U4				

REVISIONS REV	DESCRIPTION	JOB NO.	LOT QTY	LOT NO.	CODE IDENT
A	RELEASED TO RECORDS. 8-2-76				53947

PLANNER	PREP 07 DATE Bill 4/29/76	SYSTRON DONNER CORPORATION
	CHK'D	P.C. BD. ASSY., IEEE BUS CONTROL # 1A
MAT. DUE	APP'D	
B/U REQ.		SIZE B PART NO. 0515 19 02 REV A
B/U COMP	3132-0411	USED ON
		SHEET 1 OF 1

FORM E8-A 76



NOTES

1. RESISTORS ARE ¼W, 5%.
2. I.C.'s

SCH REF	TYPE	GND	VCC
U1,4	SN74LS32N	7	14
U2,15	SN74LS00N		
U3,9	SN74LS38N		
U5,11,12	SN74LS123N	8	16
U6,10	SN74LS74N	7	14
U7	SN74LS30N		
U8	SN74LS10N		
U13,14	SN74LS04N		
U16,17	MC3446P	8	16

REVISIONS				
A	RELEASE TO RECORDS	—	—	
A1			NFC	
A2		—	—	

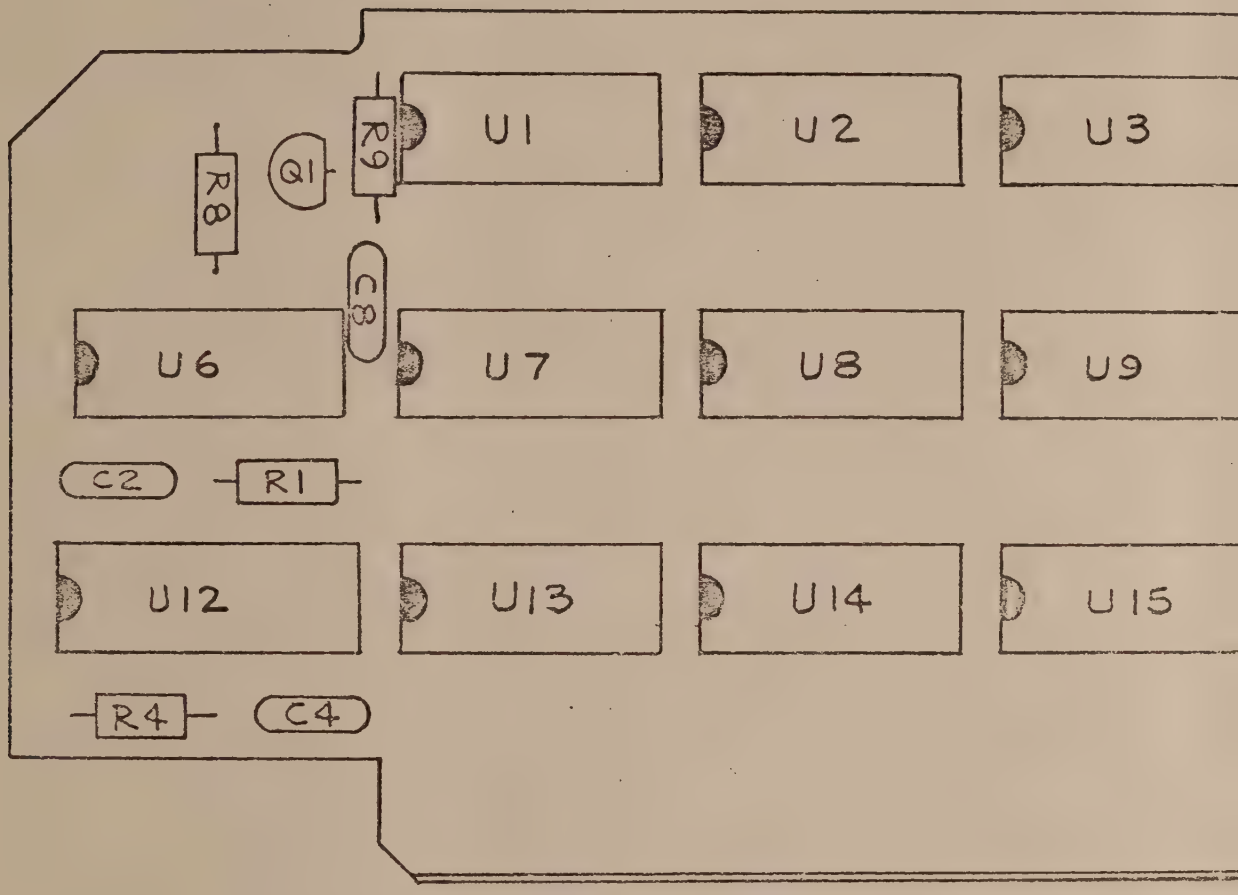
LIST OF MATERIALS

SYSTRON DONNER CORPORATION CONCORD CALIFORNIA

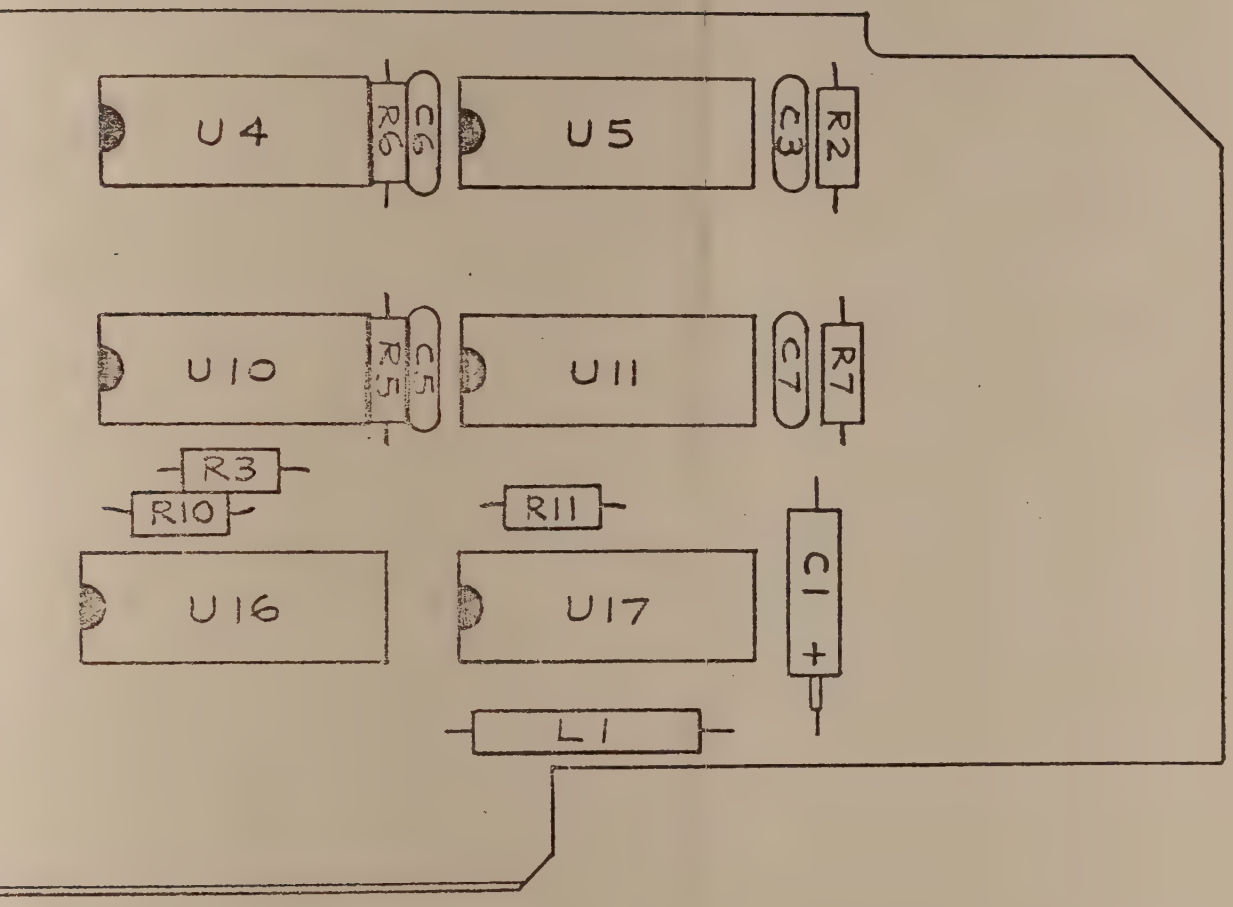
CODE IDENT 53947

IEEE BUS CONTROL ≈2

SIZE D


U1
U2
U3
R9
Q1
R8
C8
U6
U7
U8
U9
C2
R1
U12
U13
U14
U15
R4
C4

REVISIONS					
REV	DESCRIPTION	SER NO	ECO NO	DATE	APP BY
A	RELEASED TO RECORDS			7/3/74	



ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF. NO.

LIST OF MATERIALS

PROPRIETARY DATA

Furnished under United States Government Contract No. _____ Shall not be either released outside the Government or used, duplicated, or disclosed in whole or in part for manufacture or procurement, without the written permission of Systron-Donner Corporation except for (1) emergency repair or overhaul work by or for the Government, where the item or process concerned is not otherwise reasonably available to enable timely performance of the work, or (2) release to a foreign government as the interests of the United States may require, provided that in either case the release, use, duplication or disclosure hereof shall be subject to the foregoing limitations. This legend shall be marked on any reproduction hereof in whole or in part.

DRAWN	R.L.L.	DATE	7/26/73
CHECK		DATE	
ELECT.		DATE	
MECH		DATE	
PROJECT		DATE	
QA		DATE	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
DECIMAL TOLERANCE
.X ±
.XX ±
.XXX ±
ANGLES ±

SYSTRON DONNER
CORPORATION
CONCORD, CALIFORNIA

CODE IDENT 53947

P.C. BD. ASSY.
IEEE BUS
CONTROL Nº 2

MATERIAL

DRAWING NO.			
REF	SIZE	PART NO.	REV
	B	05152001	A

USED ON	NEXT ASSY
APPLICATION	

SCALE 2/1

DO NOT SCALE DRAWING

SH 1 OF 2

PARTS LIST

P.C. BOARD ASSEMBLY, IEEE BUS CONTROL #2 #05152001 REV A

REF.	DESCRIPTION	SD PART NO.
	Assembly	05152001
	Schematic	7-05152001
C1	Capacitor, 39 μF, 10 V	100183
C2,5	Capacitor, 1000 pF, D.M.	100243
C3,4,6,7	Capacitor, 330 pF, D.M.	100276
C8	Capacitor, 47 F, TANT	100186
L1	Inductor, R45-4	101313
Q1	Transistor, 2N3904	101377
R1,2,4-8	Resistor, 22 k, ¼ W	101572
R3,10,11	Resistor, 12 k, ¼ W	101565
R9	Resistor, 47 k, ¼ W	101574
U1,4	Integrated Circuit, SN74LS32N	103972
U2,15	Integrated Circuit, SN74LS00N	103130
U3,9	Integrated Circuit, SN74LS08N	103967
U5,11,12	Integrated Circuit, SN74LS123N	103976
U6,10	Integrated Circuit, SN74LS74N	103132
U7	Integrated Circuit, SN74LS30N	103971
U8	Integrated Circuit, SN74LS20N	103969
U13,14	Integrated Circuit, SN74LS04N	103749
U16,17	Integrated Circuit, MC3446	117021
	Extractor	100865

CIRCUIT DESCRIPTION
TIME OUTPUT FORMATTER
SCHEMATIC #7-05167920

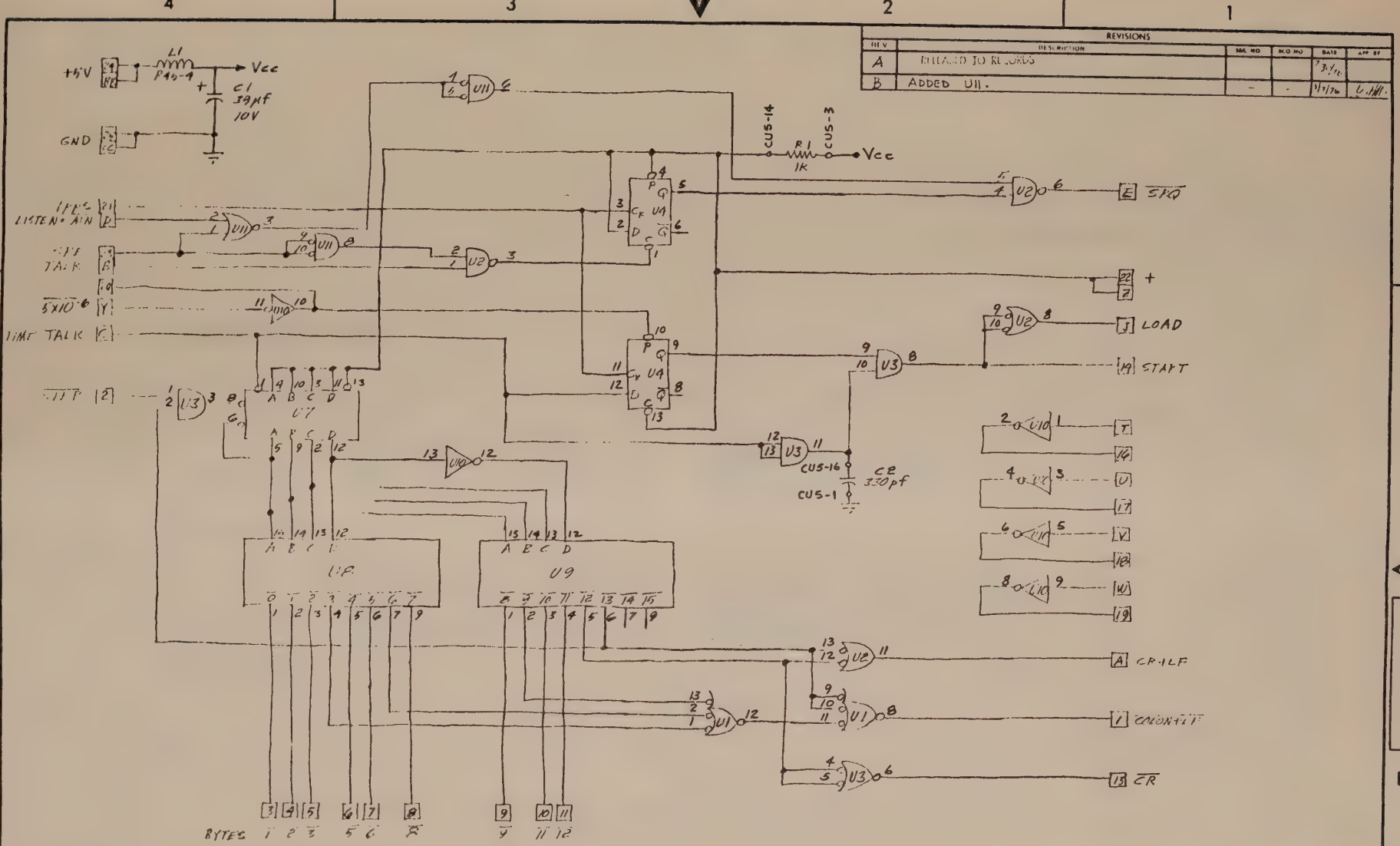
1) GENERAL

This card develops the $\overline{\text{SRQ}}$, Load and Start signals, generates the character selection signals and inverts the 8-4-2-1 bit signals from the time latches. In addition, it develops signals used to form the colon, carriage return and line feed characters in the time format.

2) CIRCUIT DESCRIPTION

When the time data sequence begins the Talk input to pin C goes high removing the count 15 preset from character counter U7 and initiating a Start via U3-11, U3-8 and pin 14. The Load output from U2-8 goes low freezing the time data in the latch buffer via pin J. The first $\overline{\text{Step}}$ input at pin 2 advances U7 to a count of "0" gating the first character onto the bus via decoder U8 and pin 3. Decoders U8 and U9 convert the binary output from U7 to 16-line. Subsequent $\overline{\text{Step}}$ inputs advance U7 through the sequence of 14 characters. Gates U1-12, U1-8, U2-11 and U3-6 select and form the colon, carriage return and line feed characters. The first four bits of each data word are fed to the Bus Control #1 Card through inverters on U10.

The $\overline{\text{SRQ}}$ output at pin E is generated at the start of each Code frame provided the unit has been designated a Listener on a Serial Poll Enable state exists. It is cleared when the unit is designated a Talker and the Serial Poll is disabled.



NOTES:

1. Resistor is ¼w, 5%.
2. IC's

U1	SN7411N	(GND – PIN 7/ Vcc – PIN 14)
U2	MC 3726P	(" " " ")
U3	MC 1000P	(" " " ")
U4	SN7474N	(" " " ")
U7	SN74LS197N	(" " " ")
U8, U9	SN7442AN	(GND – PIN 8/ Vcc – PIN 16)
U10	MC 3726P	(GND – PIN 7/ Vcc – PIN 14)
U11	MC 1810P	(" " " ")

PROPRIETARY DATA

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REVISIONS

REV	DESCRIPTION	ENG NO	MFG NO	DATE	APP BY
A	RELEASED TO RECORDS			3/1/76	
B	ADDED U11.	-	-	4/1/76	U.HH.

LIST OF MATERIALS

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

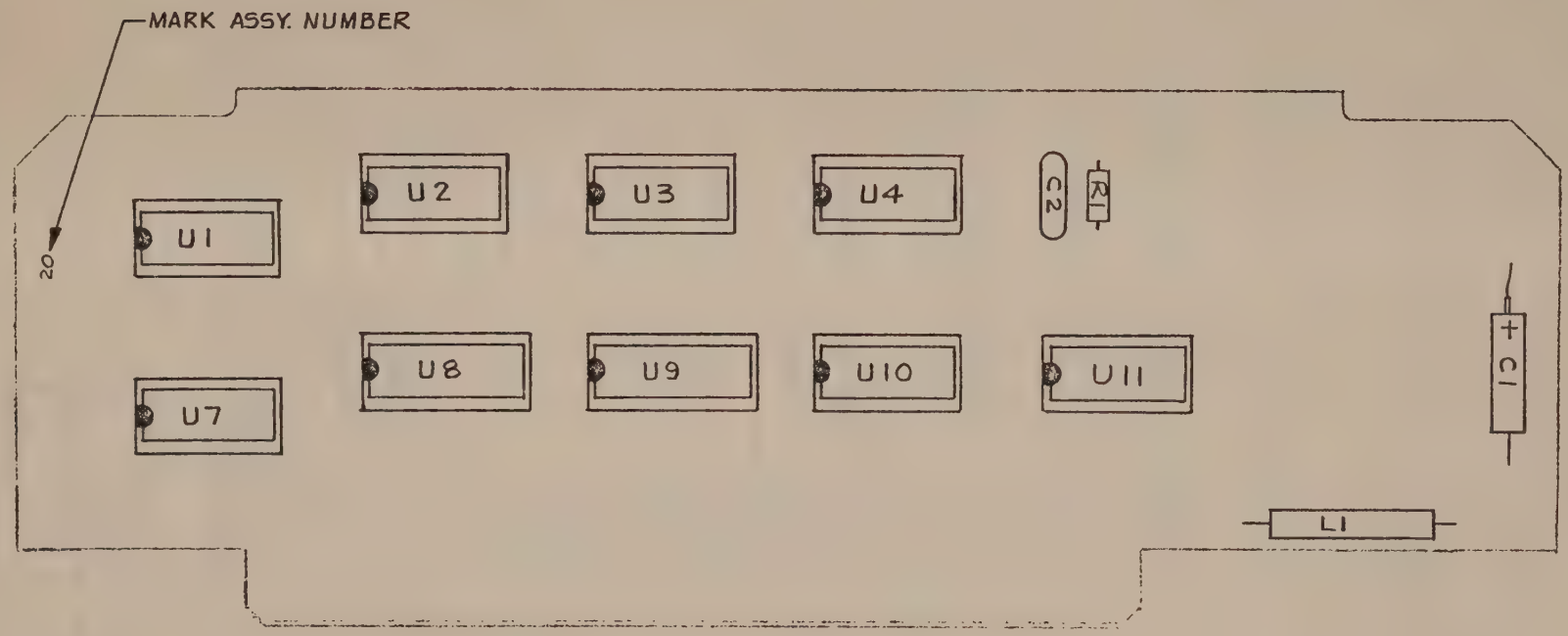
DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.1 .XX ±.01 .XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA
CHECK	DATE		CODE IDENT 53947
ELECT.	DATE		
MECH.	DATE		
PROJECT	DATE		
QA	DATE		
USED ON	NEXT ASSY		
APPLICATION			
SCALE	DO NOT SCALE DRAWING	SH 1 OF 1	
MATERIAL			

TIME OUTPUT FORMATTER

DRAWING NO. REV	SIZE	PART NO.	REV
	C	051619 20	7

P172 – 0411
P165 – 0429

B	ADDED U11.	



LIST OF MATERIALS

8155-0424
8132-0411

P.C. BD. ASSY.
TIME OUTPUT
FORMATTER

05/67920 B

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
1	D	05167920	P.C. ASSY. TIME OUTPUT FORMATTER		X			
2			SCHEMATIC	7C05167920	REF			
3	B	051679	P.C. BOARD		1			
4			P.C. BOARD ARTWORK	2DC051679	REF			
5			WIRE LIST	ACC5167920	REF			
7		100865	EXTRACTOR		2			
8		101313	INDUCTOR, R45-4	L1	1			
10		100153	CAPACITOR, 39 μf, 10V	C1	1			
11		100276	CAPACITOR, 330pf, D.M.	C2	1			
13		101569	RESISTOR, 1K, ¼W	R1	1			
15			24 GA BARE WIRE		A/R			
16			30 GA INSUL. WIRE		A/R			
18		103[illegible]	I.C. SOCKET, 14 PIN	XU1	7			
19				XU2 = SA XU1				
20				XU3				
21				XU4				
22				XU7 = SA XU1				
23		103[illegible]	16 PIN	XU8	2			
24				XU9 = SA XU8				
25				XU10 = SA XU1				
26			I.C. SOCKET	XU11 = SA XU1	1			
					1			
28		025750	INT. CKT. SN7411N	U1	1			
29		019716	MC846P	U2	1			
30		025733	MC1806P	U3	1			
31		025241	SN7474N	U4	1			
32		103[illegible]	SN74LS192N	U7	1			
33		025749	SN7442AN	U8	2			

REV	DESCRIPTION
A	RELEASED TO RECORDS. 7-30-76
A1	ITEM 32 WAS S/A U9. NOW N/C
B	ADDED XU11 & U11. 9-7-76

JOB NO. | LOT QTY | LOT NO. | CODE IDENT 53947

PLANNER | PREP DATE BILL 07/27/76 | CHK'D | APP'D | MAT. DUE | B/U REQ. 8155-0424 | B/U COMP 9320-0411 | USED ON

SYSTRON DONNER CORPORATION

P.C. BD. ASSY., TIME OUTPUT FORMATTER

SIZE D | PART NO. 05167920 | REV B

SHEET 1 OF 2

FORM E8-A 76

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
34				U9 thru U8				
35		025704	MC836P	U10	1			
36		025735	INT. CKT. MC1310P	U11	1			

REVISIONS DESCRIPTION		JOB NO.	LOT QTY	LOT NO.	CODE IDENT 53947
	PLANNER	PREP DATE	SYSTRON DONNER CORPORATION		
		CHK'D	P.C. BD. ASSY. TIME OUTPUT FORMATTER		
	MAT. DUE	APP'D			
	B/U REQ.		SIZE B	PART NO. 05167920	REV B
ECN	B/U COMP				
		USED ON	SHEET 2 OF 22		

FORM E8-A 78

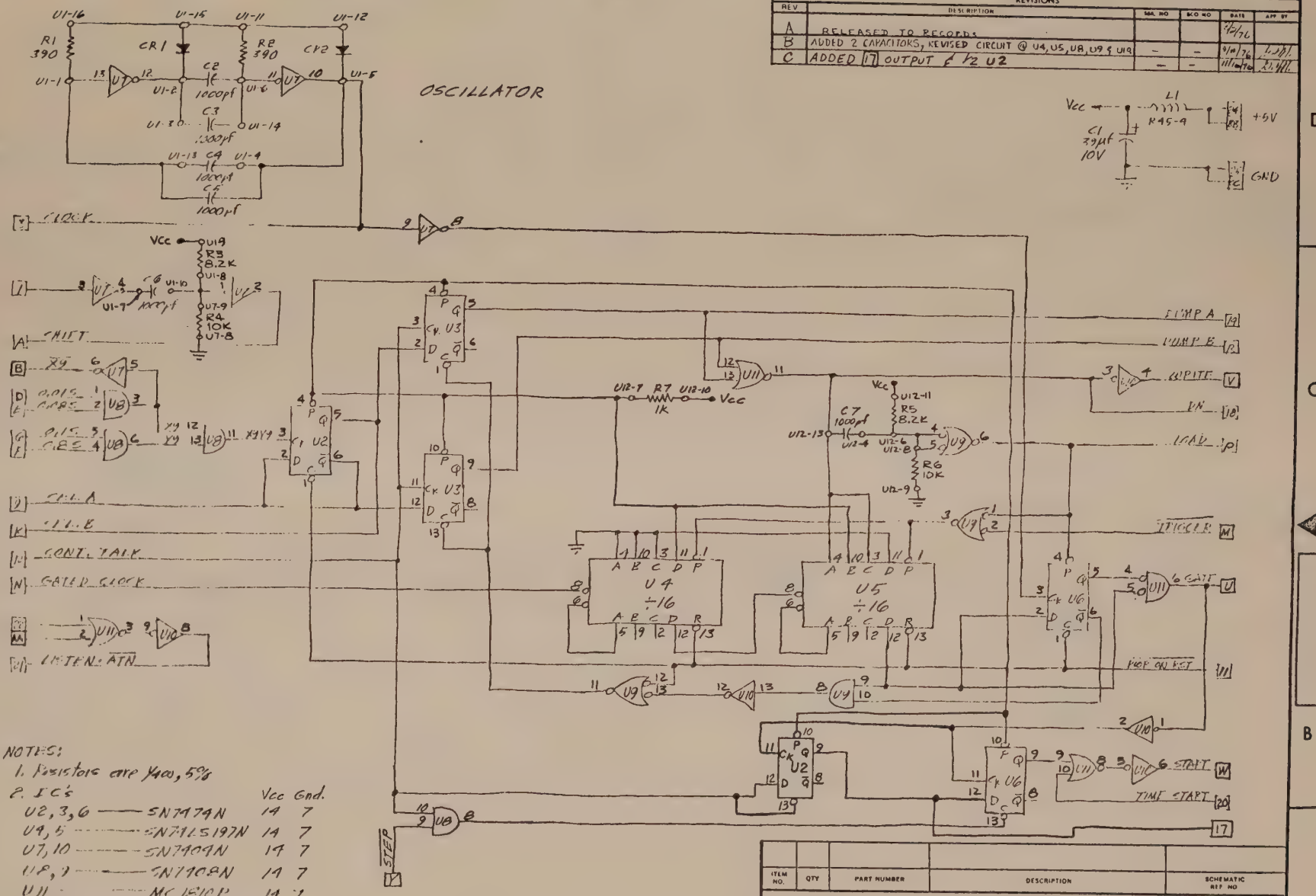
CIRCUIT DESCRIPTION
BIT COUNTER
SCHEMATIC #7-05167921

1) GENERAL

The Bit Counter selects and dumps the A and B shift registers on the Shift Register Card and clocks loading and unloading of the RAM on the Data Distributor Card.

2) CIRCUIT DESCRIPTION

Gates on U8 decode X9Y9 Code time which clocks flip-flop U2-5 producing the Sel A and Sel B signals at pins 9 and K. These signals load data from the input Code into the A and B Registers, respectively, on the Shift Register Card. When the Control Talk input to pin 12 goes high demanding data out, it sets flip-flop U3-5 or U3-9 depending on the state of U2-5. The set flip-flop outputs Dump A or Dump B (via pins 14 and R) and presets counter U4/U5 via U11-11, U9-6 and U9-3. This counter is fed Gated Clock signals from the Shift Register Card through pin N. (The Gate signal is developed at the ouput of U11-6. The Clock is generated by the Oscillator built around U6-12/10.) When precisely 88 clock pulses are counted, U5-12 goes high ending the Gate signal (and therefore the Gated Clock) and clearing the flip-flops on U3. The contents of the selected shift register are now stored in the RAM on the Data Distributor Card and counter U4/U5 is configured to count eight instead of 88 Gated Clock pulses before U5-12 goes high. The Gate at U11-6 is reestablished and the count is made each time a $\overline{\text{Trigger}}$ input via pin M is received. These groups of eight pulses shift the data in the RAM to the IEEE Bus in eight bit bytes. The signal which starts this sequence is output from U10-6 through pin W. It is developed by U6-9 when processing Control Bits and by the Data Formatter Card when processing Time Data. Flip-flop U6-9 is set when the Gate signal goes low after dumping the selected shift-register.



REVISIONS					
REV	DESCRIPTION	SRA NO	ECO NO	DATE	APP BY
A	RELEASED TO RECORDS			12/4/76	
B	ADDED 2 CAPACITORS, REVISED CIRCUIT @ U4, U5, U8, U9 & U19	–	–	9/8/76	L.D.D.
C	ADDED 17 OUTPUT & 12 U2	–	–	11/4/76	L.D.D.

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

LIST OF MATERIALS

PROPRIETARY DATA
Furnished under United States Government Contract No _____
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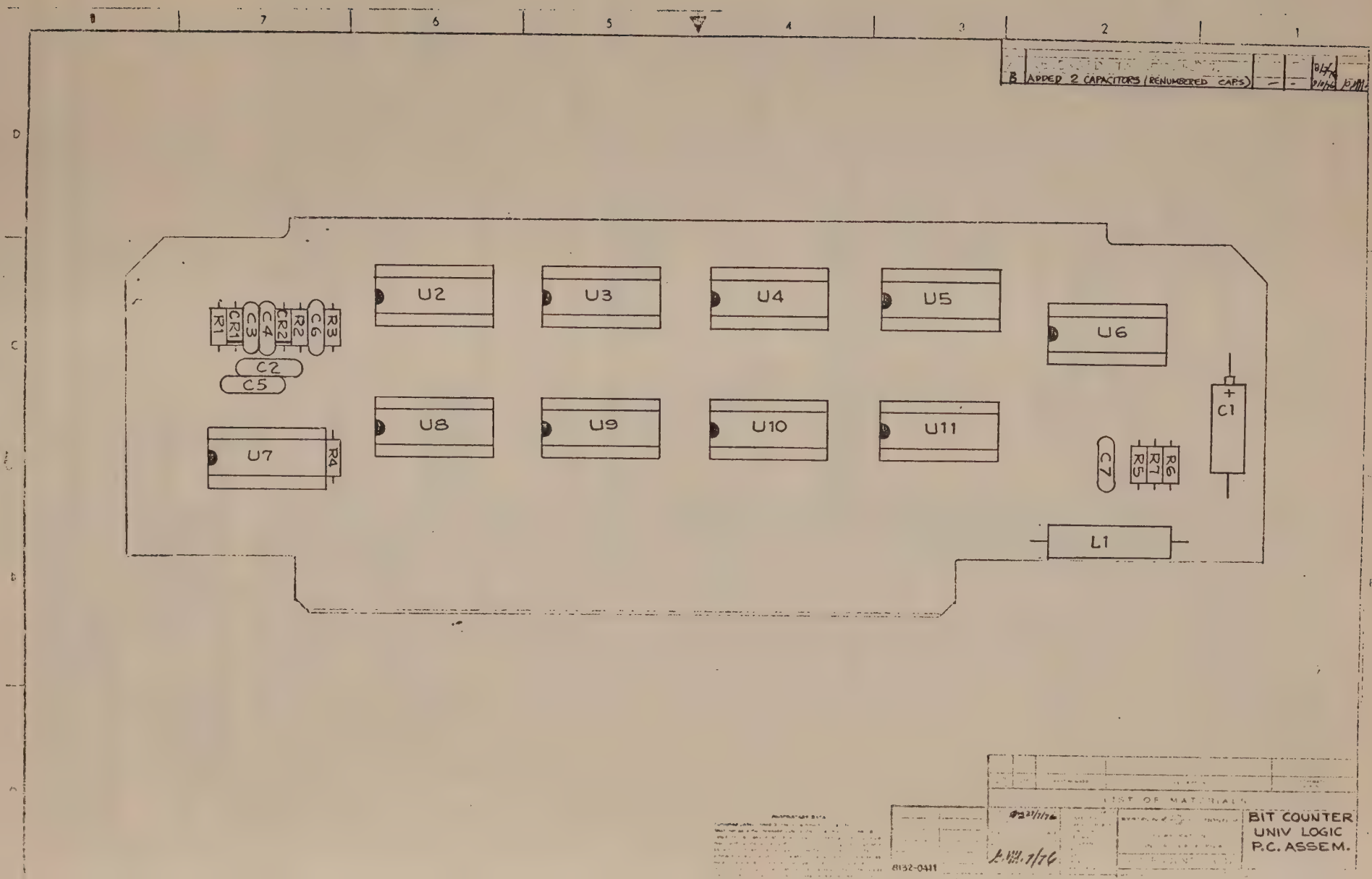
DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES	SYSTRON DONNER CORPORATION, CONCORD, CALIFORNIA
CHECK	DATE	DECIMAL	PIT COUNTER
ELECT.	DATE	TOLERANCE	
MECH.	DATE	X	CODE IDENT 53947
PRODUCTION	DATE	XX	
QA	DATE	XXX	
SCALE	DO NOT SCALE DRAWING	ANGLES ±	MATERIAL
USED ON: APPLICATION	NEXT ASSY	SH 1 OF 1	DRAWING NO. KEY 7, SIZE C, PART NO. 05167921, REV C


8 7 6 5 4 3 2 1
B ADDED 2 CAPACITORS (RENUMBERED CAPS)
U2
U3
U4
U5
U6
U7
U8
U9
U10
U11
R1
CR1
C3
C4
CR2
R2
C6
R3
C2
C5
R4
C1
C7
R5
R7
R6
L1
BIT COUNTER
UNIV LOGIC
P.C. ASSEM.
81132-0411

100243

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
1	B	05167921	ASSY		/			
2			SCHEMATIC	7C05167921	REF			
3			WIRE LIST	A05167921	REF			
4	B	051679	P.C. BOARD		1			
5			" " A/W	2D05167921	REF			
6		100365	EXTRACTORS		2			
7		100133	CAPACITOR 39μf 10V	C1	1			
8		100243	1000pf	C2	6			
9				C3 thru C2				
10				C4 " "				
11				C5 " "				
12		100365	DIODE IN4151	CR1	2			
13				CR2 thru CR1				
14		101313	INDUCTOR R45-4	L1	1			
15		101592	RESISTOR 390Ω 5% 1/4W	R1	2			
16				R2 thru R1				
17		101595	8.2K	R3	2			
18		101570	10K	R4	2			
19				R5 thru R3				
20				R6 thru R4				
21		101569	RESISTOR 1K 5% 1/4W	R7	1			
22		025241	INT CIRCUIT SN7474N	U2	3			
23				U3 thru U2				
24		103165	SN74LS197N	U4	2			
25				U5 thru U4				
26				U6 thru U2				
27		025779	SN7404N	U7	2			
28		103093	SN7403V	U8	2			
29				U9 thru U3				
30				U10 thru U7				
31		025735	INT CIRCUIT MC1810P	U11	1			
32			CAPACITOR	C6 thru C2				
33			"	C7 " "				

JOB NO. | LOT QTY | LOT NO. | CODE IDENT 53947

PLANNER | PREP DATE 2/7/76 | CHK'D | MAT. DUE | APP'D | B/U REQ. | B/U COMP | USED ON

SYSTRON DONNER CORPORATION

UNIV LOGIC P.C. ASSY

SIZE P | PART NO. 05167921 | REV B

SHEET 1 OF 2

ADDITION - TO KLEORUS 2-2-76.
ADDED 2 CAPACITORS. 9-8-76

FORM E8-A 76

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
34		103349	SOCKET, IC 14PIN DIL	XU2	10			
35				3 thru XU2				
36				4				
37				5				
38				6				
39				7				
40				8				
41				9				
42				10				
43			SOCKET	XU11 thru XU2				
44								
45								

JOB NO.	LOT QTY	LOT NO.	CODE IDENT
			53947

REVISIONS
DESCRIPTION
ECN

PLANNER	PREP DATE	SYSTRON DONNER CORPORATION
	CHK'D	UNIV LOGIC P.C. ASSY
MAT. DUE	APP'D	
B/U REQ.		SIZE P PART NO. 051679 21 REV B
B/U COMP		USED ON SHEET 2 OF 2

FORM EB-A 76

CIRCUIT DESCRIPTION
DATA DISTRIBUTOR
SCHEMATIC #7-05167922

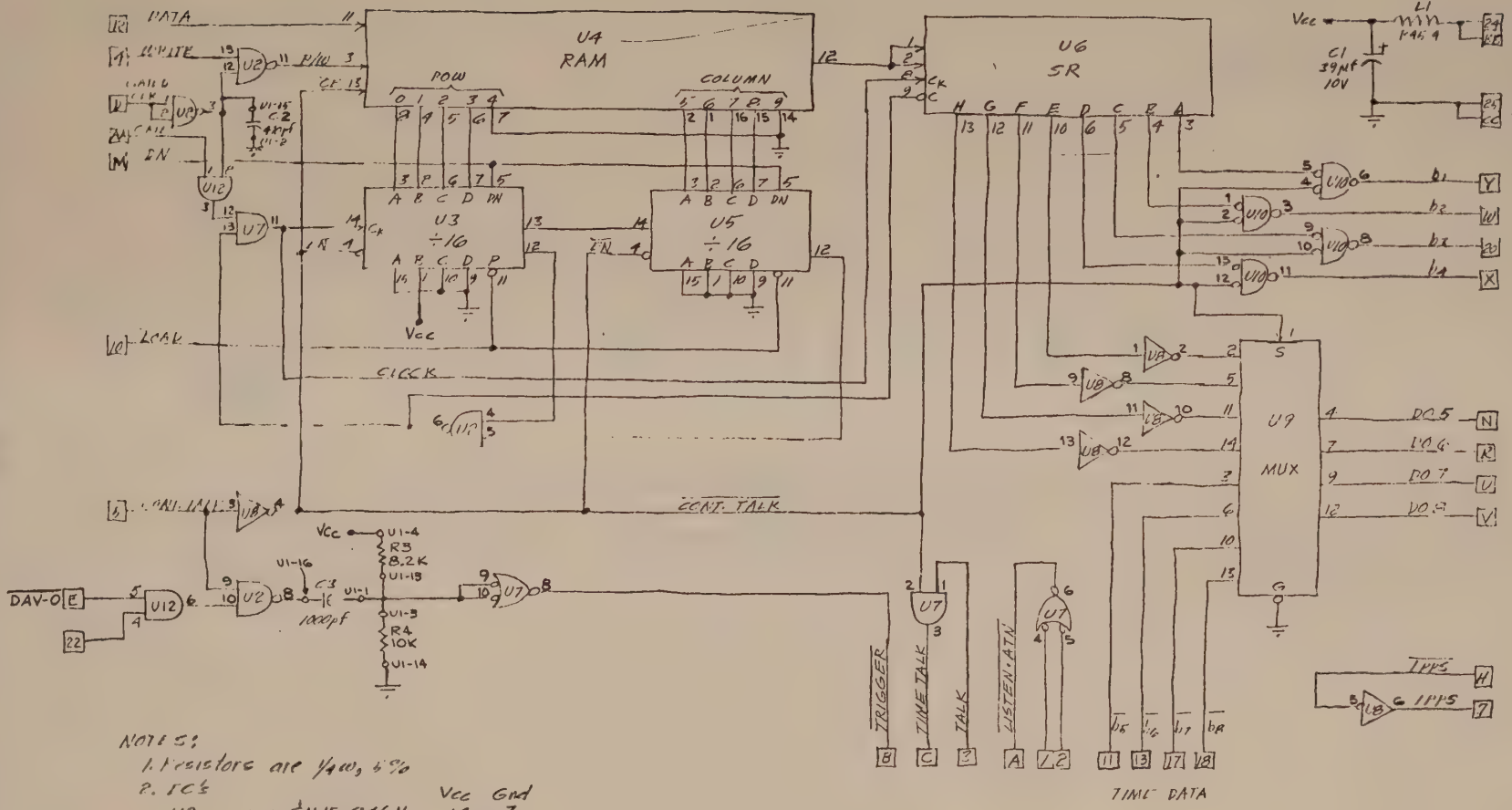
1) GENERAL

When the system is designated a Control Talker the Data Distributor accepts Control bits from the Shift Register card under control of the Bit Counter. It stores these bits in a RAM then outputs them in 8-bit bytes to the IEEE 488 Bus via the Bus Interface Cards. When the system is designated a Time Talker the Data Distributor processes ASCII zone bits from the Time Data Formatter.

2) CIRCUIT DESCRIPTION

Gated Clock pulses from the Bit Counter Card are accumulated by Counter U3/U5. During a dump operation, Counter U3/U5 is in a count up configuration. Its parallel outputs steer data from the Shift Register Card into RAM U4. Both the RAM and the Counter are enabled by the Control Talk input to pin 5. The RAM is in a write mode, Write input to pin 4 high. When the RAM is loaded, the DN input to pin M goes high placing the counter in a count down configuration, the Write input goes low and the first Trigger signal is generated by the RFD input through pin E, U2-8, U7-8 and pin B. The Counter is decremented by eight counts loading eight bits into serial in-parallel out shift register U6. These bits are output through gates on U10 and through inverters on U8 and multiplexer U9. The four low order bits from U10 are fed to the Interface through inverters on the Data Formatter Card. The high order bits from U9 are fed directly to the Interface.

REVISIONS					
REV	DESCRIPTION	MR NO	ECO NO	DATE	APP BY
A	RELEASED TO BLOCK.			3/15/76	
B	ADDED U12. U2 WAS SN7400N. C2 WAS 1000pf. DELETED R1 & R2.	–	–	9/10/76	
C	CHG'D [E] INPUT, ADDED [22] INPUT			10/6/76	



NOTES:
1. Resistors are 1/4w, 5%
2. ICs

		Vcc	Gnd
U2	SN15-B16N	14	7
U3, U5	SN74LS191N	16	8
U4	2102A-4	10	9
U6	SN74LS164N	14	7
U7, U12	SN7408N	14	7
U8	SN7404N	14	7
U9	SN74157N	16	8
U10	MC1028P	14	7

PROPRIETARY DATA

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ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

LIST OF MATERIALS

DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.1 .XX ±.01 .XXX ±.005 ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA
CHECK	DATE		
ELECT.	DATE		
MECH.	DATE		
PRODUCT ASSURANCE	DATE		
N/A	DATE		
SCALE	DO NOT SCALE DRAWING	SH 1 OF 1	MATERIAL

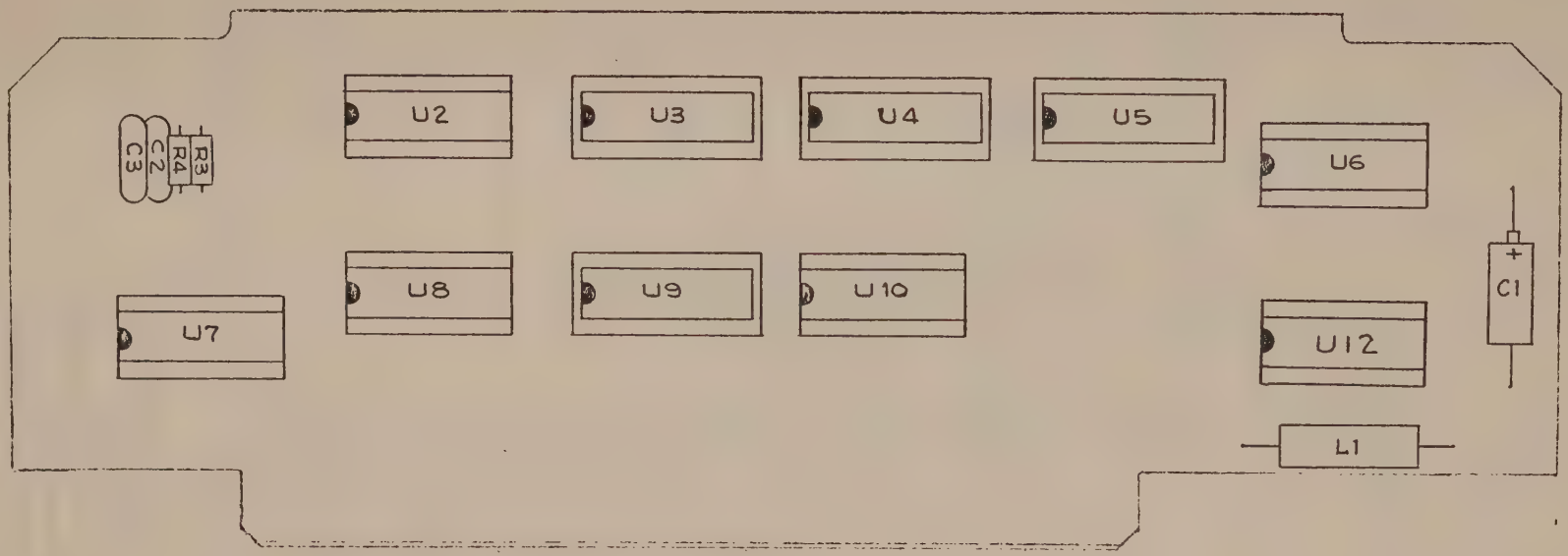
CODE IDENT 53947

DATA DISTRIBUTOR

USED ON	NEXT ASSY
APPLICATION	

DRAWING NO.			
REF	SIZE	PART NO.	REV
7	C	05167922	C

B	ADDED U12. MOVED C2. DELETED R1 & R2.	-	-	9/1/76	



8132-0411

DATA DISTRIBUTOR UNIV LOGIC ASSY

ITEM NO.	SMN	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
1		805167922	ASSY		/			
2			SCHEM	7C05167922	REF			
3			WIRE LIST	A05167922	REF			
4		05167922	P.C. BOARD		1			
5			" " A/W	2D05167922	REF			
6		100183	CAP 39Mf TANT	C1	1			
7		100221	" 470pf DM	C2	1			
8		100243	" 1000 pf DM	C3	1			
9		101313	INDUCTOR R45-4	L1	2			
10		101595	RES 8.2K 5% 1/4W	R3	1			
11		101570	" 10K " "	R4	1			
12								
13		103093	INT CKT SN7403N	U7	2			
14		019716	INT CKT SN1584% N	U2	1			
15		103982	SN74LS191N	U3	2			
* 16			2102A-4	U4	1			
17				U5		E4	13	
18		103996	SN74LS164N	U6	1			
19				U12		E4	U7	
20		025779	SN7404N	U8	1			
21		025242	SN74157N	U9	1			
22		025734	INT CKT MC1808P	U10	1			
23		103249	SOCKET IC 14 PIN DIL	XU2	6			
24		103250	16	XU3	4			
25				XU4	E4	XU8		
26				XU5	1	1 1	3	
27				XU6			2	
28				XU7			2	
29				XU8			2	
30				XU9	1	1 1	3	
31			SOCKET	XU10	E4	XU2		
32			"	XU12	"	"		
33		100365	EXTRACTOR		2			

REVISIONS REV	DESCRIPTION
A	RELEASE TO RECORDS 2-3-76
B	C7 WAS 1000 pf. U2 WAS SN7400N. DELETED R1 (8.2K) & R2 (10K). ADDED XU12 & U12. 03-03-76

JOB NO.	LOT QTY	LOT NO.	CODE IDENT
			53947

PLANNER | PREP DATE 2-27-76 | CHK'D | MAT. DUE | APP'D | B/U REQ. | B/U COMP 5132-0411 | USED ON

SYSTRON DONNER CORPORATION

UNIV LOGIC P.C. ASSY

SIZE P | PART NO. 05167922 | REV B

SHEET 1 OF 1

FORM E8-A 76

CIRCUIT DESCRIPTION
SHIFT REGISTER
SCHEMATIC #7-05167923

1) GENERAL

The Shift Register stores Control bits in two serial in-serial out shift registers under control of the Bit Counter Card.

2) CIRCUIT DESCRIPTION

Serial data stripped from the input code are loaded into the A Register (U3-U6) when Sel A is high and into the B Register (U9-U12) when Sel B is high. (There are a total of 90 Read Clock pulses from U8-3 during each load period. Each shift register contains 88 bits. The first two bits entered are shifted out and lost. These bits are the marker at X0Y0 time and 1s bit at X1Y0 time in the code. See Format.) Sel A and Sel B are high during alternate code frames, thus one is accumulating current data while the other is storing the previous frame.

When data are to be output, the Dump A or Dump B signal goes high, depending on which register is not being loaded, and the Gated Clock from U8-6 shifts the previous frame data out through pin A into the RAM on the Data Distributor Card. There are precisely 88 Gated Clock pulses during each dump. These are output from the Bit Counter Card along with the Sel A/B and Dump A/B signals.

CIRCUIT DESCRIPTION
SHIFT REGISTER
SCHEMATIC #7-05167923

1) GENERAL

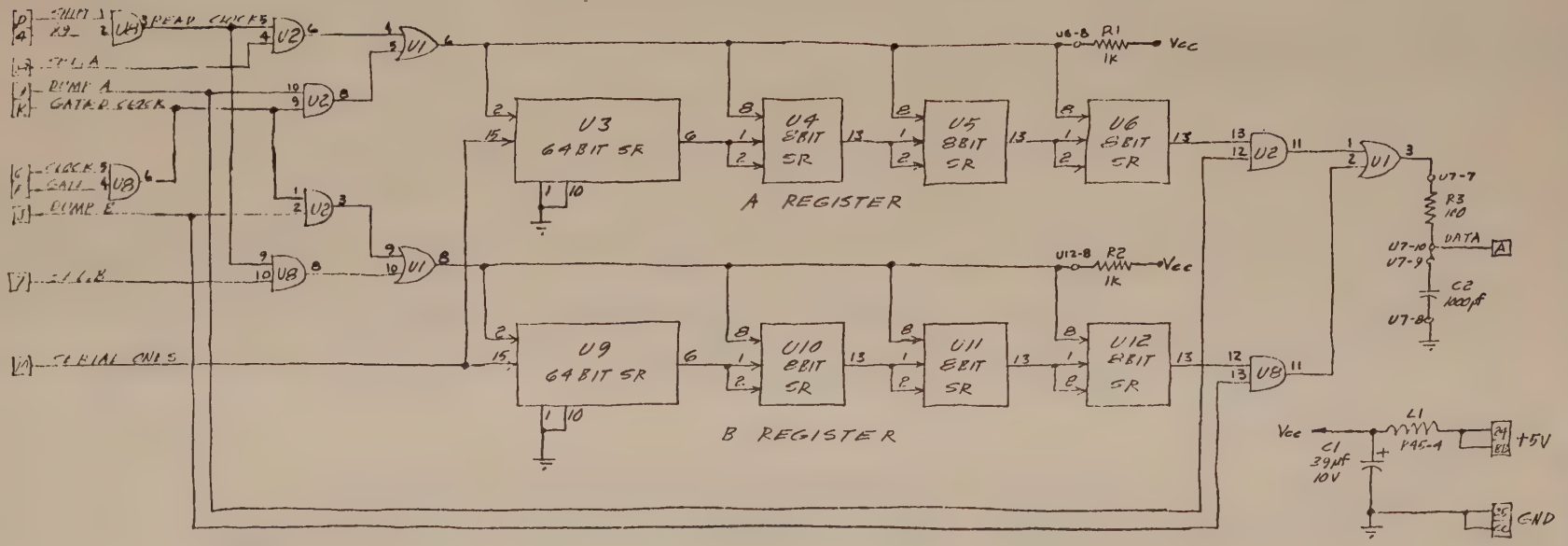
The Shift Register stores Control bits in two serial in-serial out shift registers under control of the Bit Counter Card and logic on Universal Logic Card A6.

2) CIRCUIT DESCRIPTION

Serial data stripped from the input code are loaded into the A Register (U3-U6) when Sel A is high and into the B Register (U9-U12) when Sel B is high. (There are a total of 81 Read Clock pulses from U8-3 during each load period. The logic on Card A6 blanks shift pulses at X9 times and at X4 times during Y1 through Y9. Each shift register contains 88 bits, however, only 80 bits are of interest. See Format.) Sel A and Sel B are high during alternate code frames, thus previous frame.

When data are to be output, the Dump A or Dump B signal goes high, depending on which register is not being loaded, and the Gated Clock from U8-6 shifts the previous frame data out through pin A into the RAM on the Data Distributor Card. There are precisely 88 Gated Clock pulses during each dump. These are output from the Bit Counter Card along with the Sel A/B and Dump A/B signals.

REVISIONS					
REV	DESCRIPTION	ENG NO	ECO NO	DATE	APP BY
A	RELEASED TO RECORD			8/3/72	
B	ADDED PINS 1 & 10 OF U3 & U9 TO GND, ADDED R1-3 & C2. PIN A WAS TO U1-3.			11/1/72	



NOTES:

1. IC's

		Vcc	Gnd
U1	SN7432N	14	7
U2,8	SN7408N	14	7
U3,9	CD4021AF	16	8
U4,5,6,10,11,12	SN74LS164N	14	7

ITEM NO.	QTY	PART NUMBER	DESCRIPTION	SCHEMATIC REF NO

LIST OF MATERIALS

PROPRIETARY DATA

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DRAWN	DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.XX ±.XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD CALIFORNIA
CHECK	DATE		
ELECT.	DATE		
MECH.	DATE		
PROJECT	DATE		
QA	DATE		
SCALE	DO NOT SCALE DRAWING	SH 1 OF 1	
USED ON: APPLICATION	NEXT ASSY		

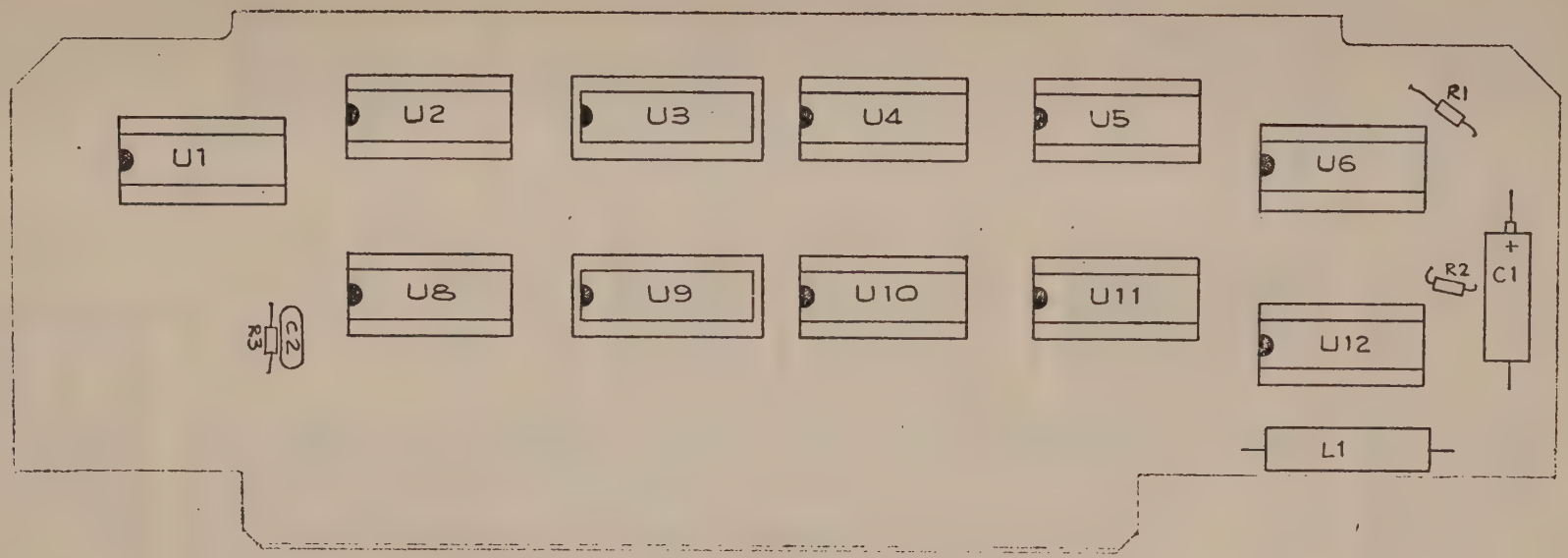
CODE IDENT. 53947

SHIFT REGISTER

MATERIAL

DRAWING NO.			
REF	SIZE	PART NO.	REV
1	C	05167923	B

B	ADDED R1-3 & C2.	-	-	8/3/76 9-7-76



0132-0411		7/7/76	SHIFT REGISTER UNIV LOGIC P.C. ASSY

23 B

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
1	B	805167923	ASSY		/			
2			SCHEMATIC	7C05167923	REF			
3			WIRE LIST	A05167923	REF			
4	3	051679	P.C. BOARD		1			
5			" " A/W	2D05167	REF			
6		100865	EXTRACTOR		2			
7		100133	CAPACITOR 39μf 10V	C1	1			
8		101313	INDUCTOR R45-4	L1	1			
9		045257	INT CIRCUIT SN7432N	U1	1			
10		103093	" " SN7408N	U2	2			
* 11			" " CD4031AE	U3	2			
* 12		10[illegible]	" " SN74LS164N	U4	6			
13				U5 thru U4				
14				U6 thru U4				
15			(NOT USED)	U7	—			
16				U8 thru 2				
17				U9 thru 3				
18				U10 thru 4				
19				U11 thru 4				
20			INT CIRCUIT	U12 thru U4				
21		103349	SOCKET IC 14PIN DIL	XU1	9			
22				12 thru XU1				
23		103350	16PIN DIL	13	2			
24				14 thru XU1				
25				15 thru 1				
26				16	1			
27			(NOT USED)	17	-			
28				18	1			
29				19	3			
30				110	1			
31				111 thru 111				
32			SOCKET	XU12 thru XU1				
33								

REVISIONS REV	DESCRIPTION
A	RELEASE TO RECORDS 2-3-76
B	ADDED R1-3 & C2. 9-7-76

JOB NO.	LOT QTY	LOT NO.	CODE IDENT
			53947

PLANNER | PREP DATE 8/28/76 | CHK'D | APP'D | MAT. DUE | B/U REQ. | B/U COMP | USED ON

SYSTRON DONNER CORPORATION

UNIV LOGIC
P.C. ASSY

SIZE P | PART NO. 051679 23 | REV B

SHEET 1 OF 2

FORM E8-A 76

PROPRIETARY DATA

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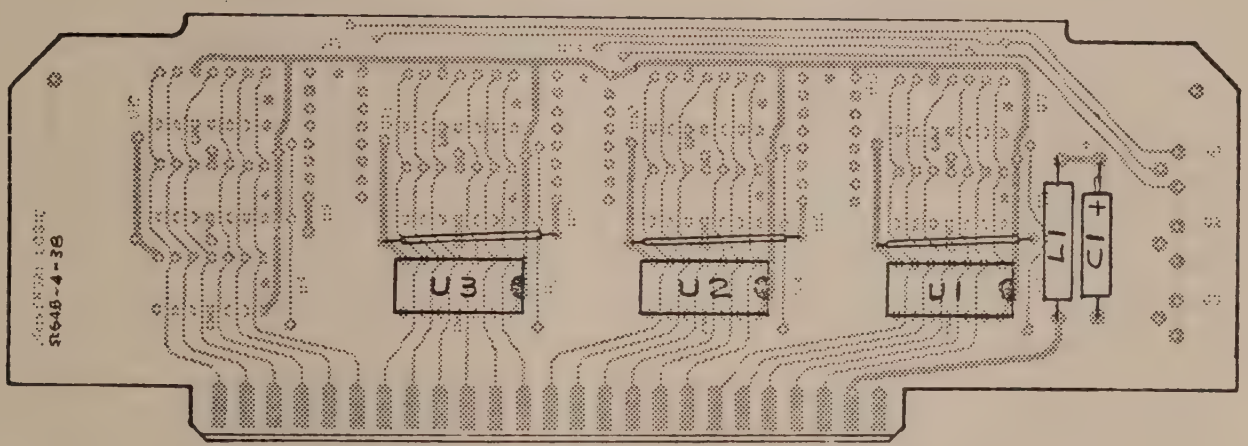
REVISIONS					
ISSUE	DESCRIPTION			DATE	APP'D
A	RELEASED TO RECORDS			12/76	



		DRAWN BLS 12-7-76 DATE	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES DECIMAL TOLERANCE .X ±.XX ±.XXX ANGLES ±	SYSTRON DONNER CORPORATION CONCORD, CALIFORNIA	UNIVERSAL LOGIC P.C. BOARD ASSY.
		CHECK DATE			
		ELECT DATE			
		MECH DATE			
		QUALITY 12/7/76			
		APPROVAL DATE			
B155-0429		SCALE 1/1	DO NOT SCALE DRAWING	MATERIAL	DWG NO 05164538 ISSUE A
USED ON	NEXT ASSY		DWG SIZE A SH 1 OF 1		
APPLICATION					

ITEM NO.	SIZE	PART NUMBER	DESCRIPTION	REFERENCE NO.	ASSY QTY	ACT. CODE	ISS. QTY	SHT QTY
1	K	05164555	ASSY	405164555	/			
3	B	051645	PC BOARD		1			
5		199163	CAP 39 uf 10V	C1	1.			
7		191303	CHOKE R45-4	L1	1			
9		02570?	IC SN7402N	U1	1			
10		01[illegible]	SN7400N	U2	1			
11		01970[illegible]	SN7410N	U3	1			
13			INSULATED JUMPER		3			

REVISIONS REV	DESCRIPTION
A	Rel to Rec 9/14/77 L E&L

JOB NO.	LOT QTY	LOT NO.	CODE IDENT
			53947

PLANNER	PREP DATE 8/17/77	SYSTRON DONNER CORPORATION
MAT. DUE	CHK'D APP'D	UNIV. LOGIC
B/U REQ.		DRAWING NO. SIZE P PART NO. 05164555 REV A
B/U COMP	532-0411 USED ON	SHEET 1 OF 1

FORM E8-A 75

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